Performance and Variation-Immunity Benefits of Segmented-Channel MOSFETs (SegFETs) Using HfO_2 or SiO_2 Trench Isolation

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Abstract—Segmented-channel MOSFETs (SegFETs) can achieve both good performance and variation robustness through the use of HfO_2 (a high- k material) to create the shallow trench isolation (STI) region and the very shallow trench isolation (VSTI) region in them. SegFETs with both an HTI region and a VSTI region (*i.e.*, the STI region is filled with HfO_2 , and the VSTI region is filled with SiO_2) can meet the device specifications for high-performance (HP) applications, whereas SegFETs with both an STI region and a VHTI region (*i.e.*, the VSTI region is filled with HfO_2 , and the STI region is filled with SiO_2) are best suited to low-standby power applications. AC analysis shows that the total capacitance of the gate (C_{gg}) is strongly affected by the materials in the STI and VSTI regions because of the fringing electric-field effect. This implies that the highest C_{gg} value can be obtained in an HTI/VHTI SegFET. Lastly, the three-dimensional TCAD simulation results with three different random variation sources [*e.g.*, line-edge roughness (LER), random dopant fluctuation (RDF), and work-function variation (WFV)] show that there is no significant dependence on the materials used in the STI or VSTI regions, because of the predominance of the WFV.

Index Terms—CMOS, tri-gate MOSFET, short-channel effect, random variation, variability

I. INTRODUCTION

Over the last few decades, extensive research has been carried out on complementary metal oxide semiconductor (CMOS) technology to achieve better performance and a higher degree of integration density in circuits. In the early days, the achievement of performance benefits was attainable simply by scaling the CMOS devices. However, after scaling devices down to sub-100-nm nodes, several technical challenges [*e.g.*, intrinsic random variations and severe short-channel effects (SCEs)] emerged, some of which seemed to be insurmountable. Many non-planar MOSFETs such as FinFETs and FDSOI MOSFETs [1, 2] have been suggested as an alternative for future CMOS scaling. Recently, the Segmented-channel MOSFET (SegFET) on a corrugated substrate with a quasi-planar tri-gate device structure was demonstrated [3-5].

The advantages and differences of the SegFET (*vs.* FinFET) are as follows: (i) the SegFET is easy for manufacture because of its lower aspect ratio of the stripes [*i.e.*, wide/short (SegFET) *vs.* narrow/tall (FinFET)] that are sufficient to suppress short-channel effects. (ii) Different from a multi-fingered FinFET in which the fingers are isolated to each other by Shallow Trench Isolation (STI), the multi-striped SegFET has the unique Very Shallow Trench Isolation (VSTI) regions in-between the stripes of equal width. The VSTI region is not the same as the conventional shallow trench isolation (STI) region. This is the reason why the fabrication of a SegFET should start onto a corrugated substrate, but the FinFET is not. (iii) The SegFET has a lower bulk punch-

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Fig. 1. Comparison of planar bulk MOSFET device structure (left) with SegFET device structure (right) (a) Isometric views, (b) plan views, (c) cross-sectional views. Note that the SegFET device structure is formed on a corrugated substrate in which each stripe is isolated by the VSTI regions (not by the STI regions).

through as well as better layout area efficiency (vs. planar bulk MOSFET). But, for FinFET, it depends on how a FinFET is designed.

In this work, a hidden device design room for the SegFET has been proposed as an evolutionary pathway for CMOS scaling. We demonstrate the n-/p-type SegFET devices on four different corrugated substrates (*i.e.*, HTI/VHTI, HTI/VSTI, STI/VHTI, and STI/VSTI substrates) whose shallow trench isolation (STI) and very shallow trench isolation (VSTI) consist of SiO₂ or HfO₂. These SegFETs on the different corrugated substrates are compared with a planar bulk MOSFET to investigate how the fringing electric-field affects the following characteristics: DC/AC device characteristics and process-induced variation immunity.

II. SIMULATION APPROACH

Fig. 1 shows the device structure of a SegFET with three identical stripes for a given 100-nm layout width, and a planar bulk MOSFET for comparison. VSTI electrically separates each stripe from the others in the channel region of the SegFET. It should be noted that the VSTI region is deeper than the source/drain extensions,

Table 1. Device Parameters for SegFET

Parameters	VALUES
Substrate type	N- or P-type
L_G	32 nm
L_{eff}	27 nm
Layout Width	100 nm
Spacer Width	27 nm
EOT	0.9 nm
H_{RECESS}	10 nm
Channel doping concentration	NMOS: $3 \times 10^{17} \text{cm}^{-3}$ PMOS: $3 \times 10^{17} \text{cm}^{-3}$
Deep S/D doping concentration	NMOS: $2 \times 10^{19} \text{cm}^{-3}$ PMOS: $3 \times 10^{19} \text{cm}^{-3}$
S/D extension doping concentration	NMOS: $1 \times 10^{19} \text{cm}^{-3}$ PMOS: $2 \times 10^{19} \text{cm}^{-3}$
X_{VSTI}	5 nm
X_{ISD}	18 nm
X_{IEXT}	7 nm
V_{DD}	1 V
Gate material	TiN
# of Stripes	3 EA

and the deep source/drain regions below the VSTI regions are electrically connected. The device width can be varied by adjusting the number of stripes. Each stripe has a quasi-planar tri-gate device structure.

To satisfy the low-standby power (LSTP) specifications in the International Technology Roadmap for Semiconductors (ITRS) [6], the device parameters of the SegFET are carefully chosen (see Table 1). As in [7], the stripe width is wider than the VSTI width in the SegFET (*i.e.*, the ratio of the stripe width to the VSTI width is 2:1), which not only improves the device performance but also suppresses both power consumption and random threshold voltage variation. Three-dimensional TCAD simulations [10] are run for the n-/p-type SegFETs with STI-HTI and VSTI-VHTI: the models involved in the simulations includes the density gradient model, drift-diffusion model, Shockley–Read–Hall recombination model, and band-gap narrowing model.

III. RESULTS AND DISCUSSION

1. DC Characteristics

i) Performance: Input Transfer Characteristics

Fig. 2 shows the input transfer characteristics of all the

Fig. 2. Input transfer characteristics of all nominal devices; (a, c) I_{DS} -versus- V_{GS} of p-type device with high/low V_{DS} , and (b, d) I_{DS} -versus- V_{GS} of n-type with high/low V_{DS} . Note that the curves are drawn both in linear and log scales.

nominal devices with high/low V_{DS} values. Note that 1.0 V and 0.05 V are chosen for high and low $|V_{DS}|$, respectively. Compared to the planar bulk MOSFET, the SegFET has a higher I_{DS} value, primarily because of the higher gate-to-channel coupling capacitance, which is increased by the quasi-planar tri-gate device structure. The drain current can be further improved when the STI region is filled with a high-k material such as HfO_2 (*i.e.*, HTI/VHTI and HTI/VSTI versus STI/VHTI and STI/VSTI) for both n-/p- type devices. This effect is mainly caused by the increased drain-to-channel capacitive coupling through the HTI regions. In high-performance (HP) applications, the HTI devices are more suitable than the STI devices. In the HTI devices, however, the off-state leakage current is increased by more than one order of magnitude, which is undesirable for satisfying the LSTP specifications. With regard to low power consumption, the STI/VHTI SegFET performs best, because it offers a relatively higher on-current, while meeting the off-state leakage requirements of LSTP. Therefore, the SegFET *per se* demonstrates flexibility in

targeted applications (*i.e.*, HP or LSTP), with the adoption of high-k materials in the STI and/or VSTI regions.

ii) Scalability: Short-Channel Effects (SCEs)

With aggressive CMOS scaling, SCEs in CMOS devices have become a huge obstacle. By scaling gate lengths from 42 nm down to 14 nm, threshold-voltage (V_{TH}) roll-off, Drain-Induced Barrier Lowering (DIBL), and sub-threshold swing degradation in both the SegFET and the planar bulk MOSFET become prominent. These effects are investigated to quantitatively evaluate the SCEs.

With L_G in the sub-25-nm scale, V_{TH} roll-off appears in both the SegFETs and the planar bulk MOSFET [Fig. 3(a)]. When compared to the planar bulk MOSFET, all the SegFET designs (*i.e.*, STI-HTI/VSTI-VHTI; total four cases) show less abrupt V_{TH} roll-off characteristics. For example, while there is a significant amount of V_{TH} roll-off in the p-type planar bulk MOSFET with a gate length of 14 nm, none of the SegFET designs shows the

Fig. 3. Short-channel effects of n/p-type devices with L_G from 42 nm down to 14 nm (a) V_{TH} roll-off curve, (b) DIBL, (c) sub-threshold swing as a function of L_G .

aforementioned V_{TH} roll-off. The V_{TH} drop in all the SegFET designs is alleviated because of the better gate controllability of the quasi-planar tri-gate device structure of each stripe in the SegFET. Minimal V_{TH} roll-off has been observed in the STI cases.

Fig. 3(b) shows the DIBL of the SegFETs and the planar bulk MOSFET. To extract DIBL values, 1.0 V and 0.05 V are chosen for the high and low drain voltage values, respectively. Compared to the planar bulk MOSFET, all the SegFETs have better DIBL

characteristics, even in the sub-25-nm regime. This would be benefited from the quasi-planar tri-gate device structure for each stripe. Among the four SegFET designs, the STI devices typically have better DIBL characteristics than the HTIs. The relatively low-k material like SiO_2 (vs. HfO_2) in the STI would induce less amount of fringing electric-field from the drain to the channel, so that the DIBL in the STI devices is alleviated. Note that the STI/VHTI device shows the least amount of DIBL.

In Fig. 3(c), the sub-threshold swing degradations of the devices are shown. As in the SCE analyses mentioned above, the SegFETs suppress sub-threshold swing degradation better than the planar bulk MOSFET, with the largest suppression in the STI/VHTI device. This would result from better gate-to-channel capacitive coupling achieved with the quasi-planar tri-gate device structure as well as less DIBL implemented with the relatively low-k material of SiO_2 . To sum up, the STI/VHTI SegFET is superior to the other devices such as STI/VSTI SegFET, HTI SegFETs, and planar bulk MOSFET, in terms of the SCEs.

2. AC Characteristics

Fig. 4 shows the gate capacitance (C_{gg}) as a function of gate voltage (V_{GS}). In the cut-off state (*i.e.*, $V_{GS} = 0$ V, at which the conductive channel is not formed), C_{gg} is highly dependent on the material used for the STI region. Two SegFETs using HfO_2 in the STI region (*i.e.*, HTI/VHTI and HTI/VSTI) have a higher C_{gg} value than both the other SegFETs and the planar bulk MOSFET. This increased C_{gg} value in the HTI SegFETs results from higher fringing electric-field effects on C_{gg} via the HTI (vs. STI) region.

As $|V_{GS}|$ increases, the conductive channel corresponding to the $|V_{GS}|$ is formed. If a non-zero V_{GS} is applied, it is likely that the fringing electric-field effect from the VSTI region will become more dominant (compared to the fringing electric-field effect from the STI region). To be more specific, the C_{gg} values of the two SegFETs using HfO_2 become more different as $|V_{GS}|$ increases. In other words, the C_{gg} value of the HTI/VHTI SegFET is higher than that of the HTI/VSTI SegFET. This difference is also observed for the two SegFETs using SiO_2 . The C_{gg} value of the STI/VHTI SegFET

Fig. 4. Gate capacitance (C_{gg}) versus gate-to-source voltage (V_{GS}) for (a) n-type devices, (b) p-type devices.

Fig. 5. The RF performance for n-type devices (right-side) and p-type devices (left-side) is evaluated: cutoff frequency (f_T) versus V_{GS} .

becomes higher than that of the STI/VSTI SegFET as $|V_{GS}|$ increases. From the C_{gg} gap observed in the cases above, it is concluded that the aforementioned C_{gg} difference is primarily caused by the larger capacitance component of the VHTI region than that of the VSTI region.

Fig. 5 depicts the dependence of cutoff frequency (f_T) on various gate voltages. Herein, note that the simplified

equation for the RF parameter is used to extract f_T value:

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (1)$$

Since C_{gg} is one of the dominant factors in determining the RF performance of devices, the curves for f_T (Fig. 5) have the similar trend with the C_{gg} curves shown in Fig. 4. It is well known that transconductance (g_m) reaches a maximum value and then decreases with increasing gate voltage. The low g_m at a high gate bias results from mobility degradation at high field. However, for the given $|V_{GS}|$ range of 0.0 ~ 1.0 V in this work, such g_m degradation is not observed. The highest f_T value for the n-type HTI/VHTI SegFET is approximately 157 GHz, while the highest f_T value for the p-type HTI/VHTI SegFET is 83 GHz. It can be explained that the reason why the f_T value for the p-type devices are lower than that for the n-type devices results from the small carrier mobility in the p-type devices which would affect the transconductance (g_m).

3. Variation-Immunity Analysis

As CMOS device sizes are reduced to a few tens of nanometers, ever-existing process-induced random variation sources are no longer negligible. Thus, three major sources of random variation in CMOS devices are investigated/compared for all the SegFET device designs (vs. planar bulk MOSFET).

i) LER (Line-Edge Roughness)

LER is defined as a measure of the roughness of the finest printed pattern edge. Fig. 6 shows the comparison of the LERs in (a) the n-type planar bulk MOSFET, (b) the n-type SegFET, (c) the p-type planar bulk MOSFET, and (d) the p-type SegFET. To quantitatively determine the LER-induced V_{TH} variation (*i.e.*, σV_{TH}), 200 different LER profiles (characterized with the correlation length of 20 nm and the RMS roughness of 2.5 nm [6]) are generated and applied to all the devices under investigation. A three-dimensional TCAD simulation for each device was run; the results are shown in Fig. 7. In contrast to the analysis of the other variation sources (*i.e.*, RDF and WFV), which will be discussed in the following sub-sections, the planar bulk MOSFET shows better

Fig. 6. Comparison of LER in (a) n-type planar bulk MOSFET, (b) n-type SegFET, (c) p-type planar bulk MOSFET, (d) p-type SegFET. The positive-/negative-sign in the scale bars under N-type doping concentration indicates the donor-/acceptor-dominant region, while the positive-/negative-sign in the scale bars under P-type doping concentration indicates the acceptor-/donor-dominant region. Note that acceptor-dominant regions are blue-colored and donor-dominant regions are red-colored for all figures above.

Fig. 7. LER-induced σV_{TH} for n-/p-type devices.

immunity to LER-induced σV_{TH} than the SegFETs. This occurs because the dominant factor in determining the LER-induced σV_{TH} value is the channel width of the device (*i.e.*, more averaging effects are to be expected with a wider channel width in the device). Note that the effective physical channel width of the SegFETs is ~ 75 nm because of the recessed silicon stripes for the given

Fig. 8. Comparison of RDF in (a) n-type planar bulk MOSFET, (b) n-type SegFET, (c) p-type planar bulk MOSFET, (d) p-type SegFET. The positive-/negative-sign in the scale bars under N-type doping concentration indicates the donor-/acceptor-dominant region, while the positive-/negative-sign in the scale bars under P-type doping concentration indicates the acceptor-/donor-dominant region. Note that acceptor-dominant regions are blue-colored and donor-dominant regions are red-colored for all figures above.

layout width, whereas the planar bulk MOSFET has a channel width of 100 nm.

ii) RDF (Random Dopant Fluctuation)

Fig. 8 shows a comparison of the RDFs in the n-/p-type planar bulk MOSFET and SegFETs. Although it is not an intentional part of device design, the doping profile of each device is random because of the RDF. The degree of the RDF is more severe in devices with a heavily-doped channel region, because the RDF-induced σV_{TH} originates primarily from the fluctuation of both the total number of dopant atoms and their position in the channel region. The effect of the RDF on the turn-on characteristics of each device under investigation is quantitatively assessed with 200 samples. Note that Sano's model [8] is chosen when randomizing the doping profiles in 3-D TCAD simulations. In Fig. 9, the smallest amount of σV_{TH} is observed in the n-/p-type STI/VHTI SegFETs. Because the use of a multiple-gate device

Fig. 9. RDF-induced σV_{TH} for n-/p-type devices.

Fig. 10. Illustration of work-function variation of (a) planar bulk MOSFET, (b) SegFET device. Note that the average grain size of TiN is 22 nm.

structure to suppress SCEs also reduces RDF-induced σV_{TH} [9], the STI/VHTI SegFET is best optimized for suppressing not only SCEs (according to Fig. 3) but also the RDF.

iii) WFV (Work-Function Variation)

Fig. 10 shows how grains are randomly shaped and distributed [10], resulting in WFV in the planar bulk MOSFET and SegFETs. Note that the average grain size of the metal gate material (*i.e.*, TiN) is 22 nm and that the grain sizes follow the Rayleigh distribution [11]. In modeling the WFV in the SegFETs, the extended gate area (EGA) [12] must be included when estimating the WFV value, because of the quasi-planar tri-gate device structure. Two-hundred samples for the WFV simulations were taken for both devices; the results are shown in Fig. 11. The SegFETs show better robustness to WFV than the planar bulk MOSFET; however, there are a few

Fig. 11. WFV-induced σV_{TH} for n-/p-type devices. Note that the gate material used for n-/p-type devices is identical.

Fig. 12. σV_{TH} induced by LER, RDF, and WFV for n-type devices (red) and p-type devices (blue).

differences in the WFV-induced σV_{TH} among the four different SegFETs. These results show that the material used in the STI and VSTI regions is not a critical factor in the WFV-induced σV_{TH} .

The total amount of σV_{TH} (Fig. 12) induced by LER, RDF, and WFV can be calculated by the equation below:

$$\sigma V_{TH}|_{Total} = \sqrt{\sigma V_{TH}|_{LER}^2 + \sigma V_{TH}|_{RDF}^2 + \sigma V_{TH}|_{WFV}^2} \quad (2)$$

The data trend in Fig. 12 is very similar to that in Fig. 11, because the WFV is the dominant factor in determining the value of σV_{TH} . In other words, (i) the effect of LER is significantly minimal because of advanced lithography technique and advanced device structure immune to short-channel effect. (ii) The effect of RDF is dramatically diminished since the channel doping concentrations in the SegFET and the planar bulk MOSFET are lower than 10^{18} cm^{-3} . Note that the RDF effect is caused primarily by the RDF in channel region [13] when its concentration is higher than 10^{18} cm^{-3} [14].

(iii) The effect of WFV is not negligible but dominant in total σV_{TH} , when the average grain size of 22 nm [11] in the metal gate material (*i.e.*, TiN) is used. Based on [11], we can simply estimate the magnitude of the WFV-induced σV_{TH} using experimentally-validated RGG concept [*i.e.*, (i) the value of the RGG for the SegFET with the EGA (Extended Gate Area) effect [12] is $0.335 \{= 22 \text{ nm} / (135 \text{ nm} \times 32 \text{ nm})^{0.5}\}$, so that the magnitude of the WFV-induced σV_{TH} for the SegFET is $40.2 \text{ mV} \{= 120 \text{ mV} \text{ (i.e., slope of TiN gate material)} \times 0.335\}$. (ii) the value of the RGG for the planar bulk MOSFET is $0.389 \{= 22 \text{ nm} / (100 \text{ nm} \times 32 \text{ nm})^{0.5}\}$, so that the magnitude of the WFV-induced σV_{TH} for the planar bulk MOSFET is $46.7 \text{ mV} \{= 120 \text{ mV} \text{ (i.e., slope of TiN gate material)} \times 0.389\}$]. These results are well matched to the TCAD simulation results, so that we can expect the reliable results by using the TCAD simulations for the WFV. Finally, it is noteworthy that the total amount of σV_{TH} induced by LER, RDF, and WFV is reasonable, as compared with previous experimental results [15].

IV. CONCLUSION

The DC/AC performance and variation-immunity benefits of the SegFETs with STI-HTI and VSTI-VHTI regions have been investigated. The HTI SegFETs' ability to have a higher on-state current is very suitable for high-performance applications. However, in LSTP applications, the STI/VHTI SegFET presents the best performance, allowing for the smallest amount of SCEs with acceptable off-state leakage current. The fringing electric-field effect has been further studied using AC characteristic analysis to obtain C_{gg} . The highest C_{gg} value was observed in the HTI/VHTI SegFET because of the enhanced fringing electric-field through high-k material of HfO_2 . Regarding random variations (*e.g.*, LER, RDF, and WFV), there was no significant dependency on the materials used in the STI or VSTI regions because of the predominance of the WFV. Therefore, the design of SegFETs for HP and LSTP applications is possible with the appropriate selection of a high-k material in the VSTI and/or STI regions.

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