Effects of Electrostatic Discharge Stress on Current-Voltage and Reverse Recovery Time of Fast Power Diode

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Abstract—Fast recovery diodes (FRDs) were developed using the $p^{++}/n/n^{++}$ epitaxial layers grown by low temperature epitaxy technology. We investigated the effect of electrostatic discharge (ESD) stresses on their electrical and switching properties using current-voltage (I-V) and reverse recovery time analyses. The FRDs presented a high breakdown voltage, >450 V, and a low reverse leakage current, $<10^{-9}$ A. From the temperature dependence of thermal activation energy, the reverse leakage current was dominated by thermal generation-recombination and diffusion, respectively, at low and high temperature regions. By virtue of the abrupt junction and the Pt drive-in for the controlling of carrier lifetime, the soft reverse recovery behavior could be obtained along with a well-controlled reverse recovery time of 21.12 ns. The FRDs exhibited excellent ESD robustness with negligible degradations in the I-V and the reverse recovery characteristics up to ± 5.5 kV of HBM and ± 3.5 kV of IEC61000-4-2 shocks. Likewise, transmission line pulse (TLP) analysis reveals that the FRDs can handle the maximum peak pulse current, $I_{pp, max}$ up to 30 A in the forward mode and down to -

24 A in the reverse mode. The robust ESD property can improve the long term reliability of various power applications such as automobile and switching mode power supply.

Index Terms—ESD, IEC 61000-4-2, TLP, fast recovery diode, carrier transport mechanism

I. INTRODUCTION

Fast recovery power diodes (FRDs) are the main part of power electronic circuits, especially, power switching circuits. In switching mode, FRDs act as a freewheeling device to protect the power semiconductors against high voltage spike damage, which is usually generated from inductance loads such as motor coils or relay windings suddenly turned "OFF". However, the FRD itself could not avoid degradation or failure due to high voltage spike, snappy recovery and electrostatic discharge (ESD) [1-4]. The p-n junction is the main structure of the FRDs, and is inevitable from the effects of ESD during the fabrication, testing, packaging and printing to board circuit process. Thus, the ESD can give a significant effect on the reliability of FRDs. Moreover, FRDs operate at high breakdown voltage, are normally more susceptible to ESD failures due to the power limited (low reverse saturation currents and high resistance value). The ESD is known as a high transient current and voltage source with a short duration time less than 150 ns, which is originated from the transfer of electrostatic charges between two objects with different electrical potentials

Manuscript received May. 18, 2014; accepted Jul. 4, 2014

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[5]. High transient voltages generated by the ESD can lead to the burn-out of the metal contact edge, surface, Si-SiO₂ interface, and p-n junction [2]. Typical damages are known as the defect states, which are the main sources of the leakage current [2, 6] and noise [7] (trapping and de-trapping of carriers in defect states, especially, at the Si-SiO₂ interface). This may also result in the degradation of the device performance as well as electrical and switching properties like the reverse leakage current, blocking voltage and reverse recovery time. Hence, the main issues involved with the effects of ESD stress on electrical and switching properties need to be addressed to guide a way of improving long-term reliability. However, almost no study is focused on investigating the effects of ESD stress on switching properties for high power FRDs. Very recently, it was reported that the Si transient voltage suppression (TVS) diodes achieved small dynamic resistance, low reverse leakage current and excellent ESD performance in excess of the IEC standard requirement (± 8 kV in contact discharge) [8-10].

In this work, Si FRDs were fabricated using low temperature epitaxy technology. Then, the influence of ESD stress on their electrical properties such as the current-voltage (I-V) and reverse recovery time (t_{rr}), were investigated in accordance with various ESD test including HBM, IEC61000-4-2 (IEC) and transmission line pulse (TLP) analysis. It will be shown that the manufactured FRDs are effective in ESD performance in conjunction with the I-V and the reverse recovery characteristics.

II. EXPERIMENTAL PROCEDURE

Fig. 1 shows the schematic of the proposed FRD with the p⁺⁺/n⁻ junction structure formed on the heavily doped n-type Si (100) substrate. First, the Si wafer was cleaned using an HF solution in order to remove impurities and native oxides. After inserting the cleaned Si wafer into a reduced-pressure chemical vapor deposition (RPCVD) chamber via a nitrogen purged load-lock chamber, it experienced high temperature hydrogen baking at 950 °C for 5 min. Then the n- type Si epitaxial layers were grown using doping gases of phosphine (PH₃). The epitaxy process was performed at low temperature (around 600-800 °C) to minimize the diffusion of dopant atoms and possible degradation of device performance

Fig. 1. Cross-section view of the proposed FRD.

caused by the non-uniform local electric field concentrated at SiO₂/Si interfaces. Linearly-graded junctions are frequently formed at high temperature for conventional drive-in processes. For forming the emitter layer, the boron implantation with a dose of 5×10^{14} /cm² was employed. In order to control the minority carrier lifetime of FRD, Pt atoms were diffused from 10 nm-thick Pt film deposited on back side n⁺⁺-substrate for 40 min at 900 - 950 °C, followed by removal of excess Pt layer. As the top electrode contact, a 2000 nm-thick Al film was deposited by means of an e-beam evaporator through the square shaped pattern with a size of 2.2×2.2 mm². The back side of substrates was grinded down to 130 μm in thickness, and followed by 100/500 nm-thick Ti/Au films for the back electrode. Current-voltage (I-V) curves and breakdown voltage measurements were performed using a parameter analyzer (Agilent 4156C) and Sony/Textronix 370 curve tracer, respectively. The ESD properties were analyzed using an ESD simulator, NoiseKenESS-6008, which can supply an output voltage of up to ± 8 kV in a human body model (HBM) and an ESS-2000 with a discharge gun TC-815R was used for the IEC61000-4-2 standard analyses. Meanwhile, TLP property was analyzed using the Barth TLP 4002 system, where the high-voltage pulse was applied step-by-step with 2 ns rise time and 100ns pulse-width. The reverse recovery characteristics were measured using the circuit diagram as shown in Fig. 2, which consists a Gwinstek GPR-30H10 and Tektronix AFG3102 as a DC power supply and pulse generation for controlling “OFF” and “ON” state of the n-channel MOSFET, respectively. The reverse recovery waveforms were captured using oscilloscope Tektronix DPO7104 equipped with TCP0030 current probe.

Fig. 2. Schematic for the reverse-recovery characterization circuit.

III. RESULTS AND DISCUSSION

The proposed FRDs rated to 400 V (avalanche breakdown at 450 V) were controlled by doping concentration and epi-layer thickness of the base layer. Generally, a high breakdown voltage diode requires wide and light base doping layer, whereas it also increases the recombination lifetime, lead to slow recovery time. In our case, we controlled the minority carrier lifetime by using the Pt diffusion instead the gold due to it implements lower temperature dependent on the reverse leakage current, fast recovery at high current operation [11] and softer recovery [12]. The Pt diffusion introduces the defect states in the band gap, acting as the minority carrier lifetime killer, which accomplish fast recovery time. The reverse recovery time, t_{rr} is the most important parameters of the power diode and general used as switching speed monitor, which defined as the total time require for depleting the storage charge at the p-n junction during turned "OFF" state. Fig. 3 plots the current and voltage waveforms captured during diode turning "off state" at various the dI_F/dt rate with controlling $I_F = 1$ A. Notable, increasing the dI_F/dt rate significantly decreases the t_{rr} from 24.8 ns and 14.6 ns while the dI_F/dt rate varies from 35 A/μs to 280 A/μs. However, undesirable the peak reverse current (I_{RRM}) increases and snappiness occur.

In order to estimate the exact t_{rr} value, $V_R = 30$ V and $I_F = 1$ A with controlling $dI_F/dt = 100$ A/μs, are widely uses to estimate the t_{rr} values of the diode in the semiconductor industries [13, 14]. As shown in Fig. 4, the reverse recovery waveform, was consistent of

Fig. 3. (a) Current, (b) voltage waveforms captured from the FRDs at various dI_F/dt rate of 35, 100 and 280 A/μs.

Fig. 4. Current and voltage waveforms of a FRD measured at $V_R = 30$ V and $I_F = 1$ A with controlling $dI_F/dt = 100$ A/μs.

negligible oscillation, this normally observe in the diode with short minority carrier lifetime as well as t_{rr} [15]. The t_{rr} and I_{RRM} were 21.12 ns and -1.54 A, respectively. Even the oscillation produced the overshoot voltage of 33.3 V or

$1.11 \times V_R$, however, it was considered as the very fast and soft reverse recovery FRD when the soft factor, S (defined as the ratio of falling time (t_f) and storage time (t_s) [12]), was 0.6. A short t_{rr} with soft reverse recovery waveform minimizes the generation of unwanted EMI and large voltage spikes in the system.

Fig. 5 shows the I-V characteristics of a FRD at various temperatures in ranging from 27 °C to 150 °C, the reverse current, I_R increases as the rising operating temperature when the carriers in semiconductor materials are followed the Boltzmann statistics. However, the reverse leakage current was kept at less 10^{-5} A.

The temperature dependence of the reverse current as given in Fig. 5, has provided a useful for investigation the effect of the Pt diffusion on the reverse leakage current conduction mechanism. For the one-side abrupt junction, the reverse current given by the Shockley equation can be expressed as [16]

$$I_R = Sq \sqrt{\frac{D_p}{\tau_p}} \frac{n_i^2}{N_D} + \frac{eSWn_i}{\tau_g} \quad (1)$$

where S is the p-n junction area, N_D is the base doping concentration, W is the depletion region width, D_p is the diffusion coefficient of hole, τ_p is the mean hole recombination lifetime and τ_g is the mean time to generate electron-hole pairs. Since $n_i \sim \exp(-E_g/2k_B T)$, the temperature dependence of the exponential terms is more stronger to than other terms. Then, the Eq. (1), can be rewritten as

$$I_R \sim \exp\left(\frac{E_g}{k_B T}\right) + \exp\left(\frac{E_g}{2k_B T}\right) \quad (2)$$

The slope of $\ln I_R - 1/k_B T$ plot is defined as the thermal activation energy (E_a) of reverse current. In principle, E_a should be close to the Si band gap (E_g) or $E_g/2$ in diffusion- or generation-recombination dominated regimes, respectively. It is well known that the generation-recombination current is mainly attributed to the carriers generated in the depletion region and dominate at low temperature. Meanwhile, the diffusion current is caused by the diffusion of minority carriers approaching the depletion edge and dominates at high temperature. The E_a values, determined from the slop of

Fig. 5. I-V characteristics of a FRD measured at various temperatures ranging from 27 °C to 150 °C.

Fig. 6. Plot of $\ln I_R$ vs. $1/k_B T$ at reverse bias of 10 V for obtaining the thermal activation energy of reverse leakage current.

$\ln I_R - 1/k_B T$ plot, were found to be 0.73 and 0.9 eV at low and high temperatures, respectively. This implies that the Pt diffusion induces the acceptor levels around 0.20 ~ 0.37 eV below the conduction band of the base Si epi-layer. Pt-induced acceptor levels calculated here are comparable to the values which were reported in a previous work [11]. Typically, the acceptor levels contribute greatly path for leakage current. However, E_a values were nearly equal to $E_g/2$ and E_g of Si, indicating the reverse leakage current of a proposed FRD was followed in principle as generation-recombination dominated at low temperature and diffusion current dominated at high temperature, which normal observe in the general p-n junction diodes.

For investigating the effect of ESD stress on the electrical and switching properties such as the reverse leakage current, breakdown voltage and t_{rr} , the FRDs

Fig. 7. I-V characteristics of the FRDs measured before and after experiencing various ESD stresses (a) HBM, (b) IEC 61000-4-2.

were also subjected to various levels of ESD pulse of 10 discharges in both positive and negative polarity with one sec time intervals. DC I-V curves and reverse recovery waveforms were measured at initially, and every time of the samples after experiencing ESD shocks to monitor the device failure. As the results, Figs. 7(a) and (b) show the I-V curves of the FRDs before and after the HBM and IEC testing, respectively. It is observed that the device was capable of withstanding up to ± 5.5 kV of HBM and ± 3.5 kV of IEC without degradations in I-V curves. However, the failure happened after ± 6 kV of HBM and ± 4 kV of IEC stressed, which observed from rapid increasing of the reverse leakage current.

Similar to the ESD stress-dependent I-V characteristics as shown in Fig. 7, the reverse recovery waveforms captured from FRDs remained unchangeable even after ± 5.5 kV of HBM and ± 3.5 kV of IEC stresses as shown in Figs. 8(a) and (b), respectively. On the other hand, after ± 6 kV of HBM and ± 4 kV of IEC applied, the

Fig. 8. Reverse recovery waveform of the FRDs measured before and after experiencing various ESD stresses (a) HBM, (b) IEC 61000-4-2.

Fig. 9. SEM images showing the damaged region by ± 4 kV IEC shocks.

devices were loosed the switching property, which correspond to the failure in I-V characteristics as shown in Figs. 7(a) and (b).

The experiment above demonstrates that the FRD cannot avoid hard breakdown and failure at high pulse voltage stress. The scanning electron microscope (SEM) picture was given in Fig. 9, reveals the cross-section

Fig. 10. TLP I-V characteristics measured from a proposed FRD.

surface of a FRD damaged by ± 4 kV of IEC shocks. The ESD shocks burnout the metal electrode and p-n junction with the depth of 74.5 μm , which could be responsible for the device failure.

Furthermore, its ESD performance was also confirmed by TLP analysis, which known as the standard ESD test in the semiconductor industries [17-20]. The TLP test results as shown in Fig. 10, reveals that the FRD was triggered ON at 0.7 V and - 450 V for the positive and negative TLP polarity, the turn-on dynamic resistance (R_{on}) obtained from a linear region were 0.03 Ω and 0.04 Ω . Typical small R_{on} value has an advantage in minimizing Joule heating, which is the major cause of device degradation and failure. The FRD could handle current up to -24 A for the negative TLP polarity and over 30 A for the positive polarity, while maintaining the reverse leakage current level as well as the original values.

As discussed above, we investigated versatile properties of the new FRDs for the first time in terms of ESD, I-V, switching characteristics. The influence of various ESD models stresses on I-V characteristics and switching properties guarantee that fabricated FRDs are high reliability and very strong ESD robustness. We believe it is crucial to address those properties for power semiconductor devices, especially in order to secure long-term reliability in harsh environments and to avoid possible serious failures.

IV. CONCLUSION

We have developed a new epitaxial FRD to be operable up to 400 V while maintaining very small reverse leakage current $< 10^{-9}$ A. The experimental data demonstrated very strong ESD robustness for the FRD to maintain in conjunction with excellent performance in I-V and switching properties. The abrupt dopant profile in the region of $p^{++}n$ junction could result in the soft reverse recovery as assisted by the reduction in carrier lifetime controlled to 21.12 ns. The FRD presented ESD protection capability as strong as ± 3.5 kV of IEC61000-4-2, ± 5.5 kV of HBM, and the $I_{pp,max}$ as measure in the TLP analysis > 30 A in the forward mode and -24 A in the reverse mode. The ESD strength may confirm useful guidelines about the long term reliability of switch power supply to be assembled with power transistors like IGBT or Power MOSFETs.

ACKNOWLEDGMENTS

This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2009-0094031), Priority Research Centers Program (2011-0031400) funded by the Ministry of Education, Republic of Korea and it was also supported by the Future Semiconductor Device Technology Development Program (Grant No. 10044651) funded By MOTIE (Ministry of Trade, Industry & Energy) and KSRC (Korea Semiconductor Research Consortium).

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