Design of a 1~10 GHz High Gain Current Reused Low Noise Amplifier in 0.18 μ m CMOS Technology

Nackgyun Seong · Yohan Jang · Jaehoon Choi

Abstract

In this paper, we propose a high gain, current reused ultra wideband (UWB) low noise amplifier (LNA) that uses TSMC 0.18 μ m CMOS technology. To satisfy the wide input matching and high voltage gain requirements with low power consumption, a resistive current reused technique is utilized in the first stage. A π -type LC network is adopted in the second stage to achieve sufficient gain over the entire frequency band. The proposed UWB LNA has a voltage gain of 12.9~18.1 dB and a noise figure (NF) of 4.05~6.21 dB over the frequency band of interest (1~10 GHz). The total power consumption of the proposed UWB LNA is 10.1 mW from a 1.4 V supply voltage, and the chip area is 0.95×0.9 mm.

Key words : Low Noise Amplifier, Low Power Consumption, Current Reused Technique, Ultra Wideband. π -Type LC Network.

I . Introduction

The ultra wideband (UWB) system is a new wireless technology that is capable of transmitting data over a wide spectrum of frequency bands with very low power consumption and high data transfer rates [1]. UWB systems are approved for use in bandwidths from 3.1 to 10.6 GHz. Different wideband pulse modulation schemes have been proposed for the UWB transmission systems, including direct-sequence systems and multiband orthogonal frequency division multiplexing systems [2~3].

One of the major challenges for both UWB systems is the design of a wideband low noise amplifier (LNA). As the first active component in the receiver chain, the LNA should provide sufficient gain and sufficiently low noise to keep the overall receiver noise figure (NF) as low as possible. In most applications, obtaining wideband input matching, good linearity, and low power consumption is desirable [4]. In addition, gain flatness over the entire frequency range of interest is necessary to meet design specifications.

The cost and integration advantages of CMOS technology have motivated extensive studies in high-speed CMOS design for wireless applications. Several CMOS LNAs with wideband characteristic and low power consumption have been proposed in recent years [5~12].

To reduce power consumption with adequate voltage gain, the current reuse technique has usually been adopted [13]. Current reused techniques can be classified into

two types. One is current reuse topology, which utilizes a two-stage cascade to share the same current source [5~8]. When the DC current is through, the circuit topology is regarded as a cascode structure, which reduces power dissipation by using the same current source. However, it requires a large chip area because additional passive components are needed. Another current reuse technique is inverter topology, which utilizes NMOS and PMOS pairs [9~12]. This technique can achieve the same NF, input impedance and overall effective transconductance with half of the power consumption required for a conventional NMOS transistor.

A current reused UWB LNA was previously discussed in [14]. It satisfies low power and compact size requirements, but does not yield adequate voltage gain and bandwidth characteristics for use as an UWB receiver. To overcome these drawbacks, we propose a 1~10 GHz high gain, current reuse UWB LNA that uses TSMC 0.18 μ m RF CMOS technology in this paper. In addition, we investigated the effect of interconnects to verify the reduction in voltage gain at high frequencies by a lumped network model of the interconnects. The proposed UWB LNA has three stages. To satisfy the wide input impedance matching and high voltage gain requirements at low power, a shunt-resistive inverter topology is utilized in the first stage. Using the cascode topology in the second stage, voltage gain in the upper frequency range can be compensated. The output stage is a source follower. Section II describes the design

principle of the proposed UWB LNA. Measured results and analysis are given in section III.

II. LNA Circuit Design

Fig. 1 shows a schematic of the proposed UWB LNA. The first stage adopts a shunt-feedback inverter topology with a source degeneration inductor. A conventional shunt-feedback topology has the drawbacks of large power consumption and gain-bandwidth trade-off. In order to improve the gain and reduce the power consumption, an inverter topology using a current reuse technique is adopted. By stacking M_2 (PMOS) on top of M_1 (NMOS), the total transconductance is increased from g_m to $g_{mN} + g_{mP}$ while retaining the same current consumption, where g_{mN} is the transconductance of M_1 and g_{mP} is the transconductance of M_2 . The resistive feedback is implemented with a current reuse technique. The feedback resistance R_f is used to extend the bandwidth and to improve the NF performance. The 3 dB bandwidth and the noise performance of the shunt-feedback inverter topology can be written as in [10],

$$BW_{-3dB} = \frac{1 + A_v}{R_f \left\{ (C_{gsN} + C_{gsP}) + (1 + A_v) \cdot (C_{gdN} + C_{gdP}) \right\}} \quad (1)$$

$$A_v \approx (g_{mN} + g_{mP}) \cdot (R_L // R_f) \quad (2)$$

$$NF \approx 1 + \frac{2}{3} \frac{1}{(g_{mN} + g_{mP})R_s} \left(\frac{1}{R_s} + \frac{R_s}{R_f^2} \right) + \frac{2}{3} \frac{(g_{mN} + g_{mP})R_s + \frac{R_s}{R_f}}{R_s} \quad (3)$$

where A_v is the open loop gain of the amplifier, R_f is the shunt feedback resistor, R_L is the load resistor of the shunt-feedback inverter topology and C_{gsN} , C_{gdN} , C_{gsP} , and C_{gdP} are the parasitic capacitances of the transistors. R_s is the impedance (50 Ω) of a source generator. Fig. 2 shows the simulated S_{11} response and noise figure with

Fig. 1. The complete schematic of the proposed UWB LNA.

Fig. 2. The proposed UWB LNA with various R_f values.

various values of feedback resistor R_f .

Flat gain over the entire bandwidth is an important factor for the UWB LNA. A peaking inductor L_g is added to obtain a flat gain characteristic at high frequencies [15] by compensating the parasitic capacitors of NMOS and PMOS. Fig. 3 shows the simulated S_{21} response with various values of inductor L_g . The large input parasitic capacitances of the first stage due to the Miller effect can lead to degradation in input impedance (below 50 Ω) and -3 dB bandwidth at high frequencies. To overcome this problem, two inductors (L_{s1} , L_{s2}) are adopted for the partial tuning-out of the input parasitic capacitances. The small signal equivalent model of the overall input stage is shown in Fig. 4. The R_{LN} and R_{LP} are the load resistors of the NMOS and PMOS transistors, respectively. When the small values of the resistances (R_{sN} , R_{sP}) and parasitic capacitances (C_{gdN} , C_{gdP}) are neglected, the input impedance of the proposed UWB LNA is given by:

Fig. 3. S_{21} response of the proposed UWB LNA with various L_g values.

Fig. 4. Small signal equivalent model of the input circuit.

$$Z_{in} = \frac{V_{in}}{I_{in}} = R_f // Z_{in,N} // Z_{in,P}, \quad (4)$$

$$Z_{in,N} = \frac{g_{mN}L_{s1}}{C_{gsN}} + j\omega(L_{s1} + L_g - \frac{1}{\omega^2 C_{gsN}}), \quad (5)$$

$$Z_{in,P} = \frac{g_{mP}L_{s2}}{C_{gsP}} + j\omega(L_{s2} - \frac{1}{\omega^2 C_{gsP}}). \quad (6)$$

To satisfy the optimum matching conditions in Eq(4), the L_g , L_{s1} , L_{s2} and the ratio of width to length of the transistor (W/L) should be selected appropriately with the proper bias condition.

In the second stage of the proposed LNA, a cascode amplifier is utilized to improve the isolation characteristic and to boost the voltage gain in the high frequency range. However, the shunt parasitic capacitances (C_{gs} of M_3 and C_{gd} of M_4) provide an additional path for the RF signal current to the ground, which then leads to voltage gain reduction especially in the high frequency band. In order to solve this problem, a π -type LC

Fig. 5. (a) π -type LC network in the second stage, (b) Smith chart.

network is added. Fig. 5(a) shows the circuit of the π -type LC network which is formed by an inductor (L_{d1}) and the parasitic capacitances. To obtain the proper inductor value of L_{d1} , we analyze the Smith chart to verify the impedance using Advanced Design System 2005A, as shown in Fig. 5(b). The optimum value of L_{d1} is 3.07 nH. A series peaking inductor L_{d2} resonates with the total parasitic capacitance of the transistor M_6 to provide additional bandwidth. The output stage is a source follower. The proposed schematic can provide high gain with low power consumption.

III. Measurement Results

The proposed UWB LNA is implemented using Cadence SpectreRF [16] with TSMC 0.18 μm RF CMOS technology. As shown in Fig. 6, the chip size is mainly determined by the sizes of the on-chip spiral inductors. The total chip area is 0.95×0.9 mm, including the measurement pads. The measurement results were obtained using a GSG probe station, combined with an Agilent 8510C network analyzer and an Agilent E4407B NF meter. Fig. 7 shows the measured S -parameters and NF of the proposed UWB LNA. A 10 dB return loss bandwidth is sufficient to cover the frequency band from 1 GHz to 10 GHz. The measured NF ranges from 4.05 to 6.21 dB over the entire frequency band. The stability factor is calculated using the measured S -para-

Fig. 6. Microphotograph of the proposed UWB LNA (Size of 0.95×0.9 mm).

Fig. 7. Measured and simulated S-parameters and NF of the proposed UWB LNA.

meters and its value is greater than 1 across the desired bandwidth. The input-referred 1-dB compression point (P_{1dB}) is -15.2 dBm and the input-referred third-order intermodulation point (IIP3) is -4 dBm at 5.5 GHz. The P_{1dB} and IIP3 over the frequency band are plotted in Fig. 8. The measured voltage gain reaches its maximum value of 18.1 dB at around 1 GHz and this is about 5.5 dB lower than the simulation at high frequencies, due to parasitic effects. Since circuit performance is affected by interconnects, we investigated the effect of interconnects to verify the reduction in voltage gain at high frequencies [17]. In order to include the interconnect effects in the simulation, interconnects are represented by a lumped network model, as shown in Fig. 9 [18]. The variables L_s and R_s represent the series inductance and resistance, respectively. L_{sk} and R_{sk} represent the inductance and resistance arising from skin effects and are dependent on operating frequencies, and C_{ox} , R_{sub} , and C_{sub} are the oxide layer capacitance, substrate resistance, and capacitance, respectively. These

Fig. 8. The P_{1dB} and IIP3 over the frequency band.

Fig. 9. Lumped network modeling of the interconnect.

parameters are extracted from calculated Y-parameters. From Fig. 9, Z_{series} is given by:

$$Z_{series}(\omega) = R_s + \frac{\omega^2 L_{sk}^2 R_{sk}}{R_{sk}^2 + \omega^2 L_{sk}^2} + j\omega L_s + \frac{j\omega L_{sk} R_{sk}^2}{R_{sk}^2 + \omega^2 L_{sk}^2} \quad (7)$$

and is equal to $1/Y_{series} = -1/Y_{21}$. Z_{shunt} is given by:

$$Z_{shunt}(\omega) = \frac{R_{sub}}{1 + \omega^2 C_{sub}^2 R_{sub}^2} + \frac{1 + \omega^2 C_{sub} R_{sub}^2 (C_{ox} + C_{sub})}{j\omega C_{ox} (1 + \omega^2 C_{sub}^2 R_{sub}^2)} \quad (8)$$

and the shunt impedance (Z_{shunt}) is equal to $1/Y_{shunt} = 1/(Y_{11} + Y_{21})$. Therefore, using the simulated values of Y_{11} and Y_{21} , together with Eqs. (7) and (8), the series and shunt effective parasitic parameters depending on the frequencies, can be extracted. Fig. 10 compares the voltage gain of the schematic circuit, the modified voltage gain including the interconnect effects, and the measured voltage gain. The modified simulation results are close to the measured ones, as shown in Fig. 10. A performance summary of the proposed UWB LNA is listed in Table I and compared with those of previously designed current reuse CMOS UWB LNAs. In addition, the figure of merit (FOM) given by [19]:

$$FOM = \frac{Gain_{max dB} BW_{3dB GHz}}{NF_{min dB} P_{dW}} \quad (9)$$

Table 1. Performance summary and comparison to with other UWB CMOS LNAs.

Reference	Simulated [6]	Measured [7]	Measured [8]	Measured [9]	Measured [10]	Measured [11]	Measured [12]	Measured [20]	Measured This work
Technology	0.18 μm RF CMOS	0.18 μm RF CMOS	0.18 μm RF CMOS	0.18 μm RF CMOS	0.13 μm RF CMOS	0.09 μm RF CMOS	0.18 μm RF CMOS	0.18 μm RF CMOS	0.18 μm RF CMOS
Bandwidth [GHz]	3.1~10.6	3.1~10.6	2.7~8.2	2~9	2~9	0.1~20	3.1~10.6	2.7~6.2	1~10
S_{11} , S_{22} [dB]	<-8.7	<-8	<-8	<-8.5	<-10	<-10	<-11	<-9	<-10
Gain _{max} [dB]	13.1	16	14.2	13.5	11.5	12.7	11.5	10	18.1
NF [dB]	2.7~4.9	3.1~6	4.1~6.8	2.5~7.4	4.45~9	3.3~5.5	4.5~5.1	3.1~7.8	4.05~6.21
IIP3 [dBm]	-9	-7*	-	-5.4	-	-2.5***	-12	-0.2	-4
Power [mW]	13.9	11.9	7.2	25.2	17**	12.6	9	8.3	10.1
Area [mm ²]	-	1.2	0.78	0.87	0.6	0.35	0.46	0.8	0.85
FOM	2.61	3.25	3.16	1.18	1.10	6.1	2.13	1.41	3.94

* at 6 GHz, ** only core, *** average

Fig. 10. Comparison of the voltage gains.

is higher than those of the other UWB LNAs. The total power consumption of the proposed LNA is 10.1 mW.

IV. Conclusion

In this paper, we propose a high gain, current reuse CMOS UWB LNA. In order to obtain a high transconductance with low power consumption, a shunt-resistive inverter topology with a peaking inductor was used in the first stage. The π -type LC network technique was also adopted in the second stage to achieve a sufficient flat gain over the entire frequency band. The total power consumption of the proposed LNA is 10.1 mW from a 1.4 V supply voltage. The results show that the proposed design methodology is suitable for an UWB LNA design. Further research on gain reduction issues at high is still needed.

This research was supported by the MKE (Ministry of Knowledge Economy), Korea, under the ITRC (Information Technology Research Center) support program supervised by the IITA (Institute of Information Technology Assessment).

References

- [1] FCC, "Final rule of the Federal Communications Commission, 47 CFR Part 15, Sec. 503," *Federal Register*, vol. 67, no. 95, May 2002.
- [2] DS-UWB Physical Layer Submission to 802.15 Task Group 3a, [Online]. Available: <ftp://ftp.802wirelessworld.com/15/04/15-04-0137-03-003a-merger2-proposal-ds-uwv-update.doc>.
- [3] Multi-Band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a, [Online]. Available: ftp://ftp.802wirelessworld.com/15/Archive/2003/Jul03/03268r3P802-15_TG3a-Multi-Band_CFP-Documents.doc.
- [4] Aly Ismail, Asad A. Abidi, "A 3~10-GHz low-noise amplifier with wideband LC-ladder matching network," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2269-2277, Dec. 2004.
- [5] Z. D. Huang, Z. M. Lin, and H. C. Lai, "An high gain low noise amplifier with current-reused technique for UWB applications," *IEEE Conference on Electron Devices and Solid-State Circuits, Proc.*, pp. 977-980, Dec. 2007.
- [6] Zhe-Yang Huang, Che-Cheng Huang, Yeh-Tai Hung, and Meng-Ping Chen, "A CMOS current reused low-noise amplifier for ultra-wideband wireless recei-

- ver," *International Conference on Microwave and Millimeter Wave Technology, Proc.*, pp. 1499-1502, Apr. 2008.
- [7] Yi-Jing Lin, S. S. H. Hsu, Jun-De Jin, and C. Y. Chan, "A 3.1~10.6 GHz ultra-wideband CMOS low noise amplifier with current-reused technique," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 3, pp. 232-234, Mar. 2007.
- [8] Shou-Chien Huang, Cheng-Hsiu Tsai, and Yue-Ming Hsin, "Low power consumption and high gain ultra wideband low noise amplifier," *Microwave and Optical Technology Letters*, vol. 51, no. 2, pp. 382-384, Feb. 2008.
- [9] C. W. Kim, M. S. Jung, and S. G. Lee, "Ultra-wideband CMOS low noise amplifier," *IET Electronics Letter*, vol. 41, no. 7, pp. 384-385, 2005.
- [10] T. Taris, J. B. Begueret, and Y. Deval, "A low voltage current reuse LNA in a 130 nm CMOS technology for UWB applications," *European Microwave Integrated Circuit Conference, Proc.*, pp. 307-310, Oct. 2007.
- [11] M. Chen, J. Lin, "A 0.1~20 GHz low-power self-biased resistive-feedback LNA in 90 nm digital CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 5, pp. 323-325, May 2009.
- [12] Chang-Tsung Fu, Chien-Nan Kuo, and Stewart S. Taylor, "Low-noise amplifier design with dual reactive feedback for broadband simultaneous noise and impedance matching," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 4, pp. 795-806, Apr. 2010.
- [13] H. Fouad, K. Sharaf, E. El-Diwany, and H. El-Hennawy, "An RF CMOS cascode LNA with current-reuse and inductance source degeneration," *Radio Science Nineteenth National Conference, Proc.*, pp. 450-457, 2002.
- [14] N. G. Seong, Y. H. Jang, and J. H. Choi, "Design and analysis of a compact ultra wideband CMOS low noise amplifier," *Microwave and Optical Technology Letters*, vol. 53, no. 2, pp. 345-348, Feb. 2011.
- [15] Shih-Fong Chao, Jhe-Jia Kuo, Chong-Liang Lin, Ming-Da Tsai, and Huei Wang, "A DC-11.5 GHz low-power, wideband amplifier using splitting-load inductive peaking technique," *IEEE Microwave And Wireless Components Letters*, vol. 18, no. 7, pp. 482-484, Jul. 2008.
- [16] Spectre Circuit Simulator, Cadence Design Systems, INC., www.cadence.com
- [17] B. Kleveland, X. Qi, Madden, T. Furusawa, R. W. Dutton, M. A. Horowitz, and S. S. Wong, "High frequency characterization of on chip digital interconnects," *IEEE Journal of Solid-State Circuits*, vol. 37, issue 6, pp. 716-725, Jun. 2002.
- [18] Xiaomeng Shi, Jianguo Ma, Beng Hwee Ong, Kiat Seng Yeo, Manh Anh Do, and Erping Li, "Equivalent circuit model of on-wafer interconnects for CMOS RFICs," *IEEE Radio and Wireless Conference, Dig.*, pp. 95-98, Sep. 2004.
- [19] R. M. Weng, P. C. Lin, "A 1.5 V low-power common-gate low noise amplifier for ultra wideband receivers," *IEEE International Symposium Circuits and Systems 2007, Dig.*, pp. 2618-2621, May 2007.
- [20] Jeong-Yeon Kim, Chang-Wan Kim, "A 0.18- μ m CMOS UWB LNA combined with high-pass-filter," *Journal of the Korean Institute of Electromagnetic Engineering and Science*, vol. 9, no. 1, Mar. 2009.

Nackgyun Seong

was born in Incheon, Korea, in 1984. He received the B.S. degree from Myongji University, Gyeonggi, Korea, in 2009, and is currently working toward the M.S. degree at Hanyang University. His research interests include RF transceiver front-end circuit design and antenna design.

Yohan Jang

was born in Seoul, Korea in 1977. He received the B.S. degree from Kwangwoon University, Seoul, Korea, in 2003. He was researcher of bluetooth hardware department at Youngbo Engineering from 2003 to 2005. He is currently working toward the Unified course of the M.S. and the Ph.D. degree at Hanyang University. His research interests include CMOS RFIC design, wireless power transfer design and microwave active device design.

Jaehoon Choi

was born in Seoul, Korea, in 1957. He received the B.S. degree from Hanyang University, Korea, the M.S. degree and the Ph.D. degree from Ohio State University, Ohio, in 1980, 1986 and 1989, respectively. From 1989~1991, he was a research analyst with the Telecommunication Research Center at Arizona State University, Tempe,

Arizona. He had worked for the Korea Telecom as a team leader of the Satellite Communication Division from 1991 to 1995. Since 1995, He has been a professor in the Department of Electrical and Computer Engineering at Hanyang university, Korea. He has published more than 100 refereed journal articles and numerous conference proceedings. He also holds 20 patents. His research interests include antenna, microwave circuit design, and EMC. Currently, his research is mainly focused on the design of compact, multiband antenna for mobile wireless communication, software defined radio (SDR) systems and ultra wideband (UWB) systems.