A Lock-Time Improvement for an X-Band Frequency Synthesizer Using an Active Fast-Lock Loop Filter

Yun-Seong Heo · Hyun-Seok Oh · Hae-Chang Jeong · Kyung-Whan Yeom

Abstract

In phase-locked frequency synthesizers, a fast-lock technique is frequently employed to overcome the trade-off between a lock-time and a spurious response. The function of fast-lock in a conventional PLL (Phased Lock Loop) IC (Integrated Circuit) is limited by a factor of 16, which is usually implemented by a scaling of charge pumper, and consequently a lock time improvement of a factor of 4 is possible using the conventional PLL IC. In this paper, we propose a novel external active fast-lock loop filter. The proposed loop filter provides, conceptually, an unlimited scaling of charge pumper current, and can overcome conventional trade-off between lock-time and spur suppression. To demonstrate the validity of our proposed loop-filter, we fabricated an X-band frequency synthesizer using the proposed loop filter. The loop filter in the synthesizer is designed to have a loop bandwidth of 100 kHz in the fast-lock mode and a loop bandwidth of 5 kHz in the normal mode, which corresponds to a charge pumper current change ratio of 400. The X-band synthesizer shows successful performance of a lock-time of below 10 μ sec and reference spur suppression below -64 dBc.

Key words: Active Fast-Lock Loop Filter, Lock-Time, Spurious Suppression, Charge Pump Current.

1. Introduction

A frequency synthesizer is frequently used as a signal source, and is regarded as an essential device in communication systems. Its frequency can be synthesized using the control signals from a program in a personal computer. Various implementations for frequency synthesizers are proposed [1]. One of them is using PLL (Phase Locked Loop), which is based on frequency divider. Fig. 1 shows a typical block diagram of our frequency synthesizer using frequency dividers. In comparison to a conventional frequency synthesizer, a divider of 1/4 is internally built in a voltage controlled oscillator (VCO) IC. In Fig. 1, a desired reference frequency or frequency channel step (f_{CH}) is generated, dividing the reference frequency (f_{ref}) by R counter. Then, after locking, a frequency of VCO is determined by

$$f_{VCO} = 4N \times f_{CH} = 4N / R \times f_{ref} \quad (1)$$

where N is division ratio of VCO frequency. Thus, the frequency of VCO can be synthesized with a step frequency f_{CH} by changing the value of N .

The important figures of merit in this type of frequency synthesizer are lock-time and reference spur suppression, which are critically dependent on the loop filter bandwidth. As a loop bandwidth increases, lock-time

Fig. 1. A frequency synthesizer implemented by a divider.

is decreased but spurs increase. Conversely, when a loop bandwidth decreases, spurs are suppressed but lock-time increases.

Such trade-off makes it difficult to implement the loop filter to yield both a satisfactory fast lock-time and spur suppression. However, recent communication and military applications require more stringent spectral purity of signal sources, with faster settling time.

To address this trade-off between settling time and loop bandwidth, several works were introduced [2]~[6]. One design approach is to utilize a pre-determined look-up table to adjust the output frequency immediately [5], [6]. The lookup table initially records the proper frequency-setting configurations for all channels. When the PLL is commanded to change its frequency to a certain

channel, the configuration stored in the lookup table is loaded to the PLL and sets the voltage-controlled oscillator (VCO) to the desired output frequency. A short settling time can be achieved since the output frequency is directly set. However, it is difficult to generate an accurate lookup table, since the frequency-setting configuration for each channel is sensitive to process, voltage, and temperature variations. Consequently, this approach often requires complex calibrations to realize such a lookup table [5]. Bandwidth switching is another useful technique for decreasing the settling time [2]~[4]. The main idea of this approach is to widen the loop bandwidth during locking and then change the bandwidth to the desired narrow one when the loop reaches a locked state. Since the loop is switched to a wide loop bandwidth before the locked state, this method somewhat assimilates the capability of the locking speed of a wide-bandwidth PLL. The realization of a switchable loop bandwidth is straightforward. The bandwidth can be enlarged by increasing the charge pump current. Meanwhile, the loop damping factor should be maintained for preserving the loop dynamics and stability. The improvement in locking speed is determined by the expanding ratio of the loop bandwidth, which is often limited by practical implementation considerations [2].

Recently, such a fast-lock technique has been suggested for commercial PLL IC [7] to overcome this trade-off. A fast-lock technique is the way to satisfy both lock-time and spur suppression through two mode operations with mode dependent phase detector constants.

When PLL is in an unlocked state, a larger phase detector constant is set, and a loop filter can quickly achieve a locked state. Such mode is called a fast-lock mode. In contrast, when the loop is in a locked state, a smaller phase detector constant is set, and a loop filter provides sufficient suppression of spur leakage. This mode is called normal mode. In conventional PLL ICs, a phase detector is implemented by charge pumper current source, and consequently the fast-lock technique is achieved by altering charge pumper current. The ratio of phase detector constant in conventional ICs is limited by 16, which results in loop bandwidth ratio to 4. Thus, lock-time can be improved by a factor of 4 at most faster than that in normal mode. Furthermore, the improvement in spur suppression is limited about 17 dBc, which corresponds to a factor of 4. As a result, it is impossible to achieve additional lock-time improvement and spur suppression above a factor of 4.

In this paper, we propose a novel active loop filter to provide not only faster lock-time but also sufficient spur suppression. This is realized by the loop filter circuit that can drastically improve the change ratio of the

phase detector constant. To verify our loop filter, an X-band frequency synthesizer is fabricated. With the proposed loop filter, the synthesizer demonstrates a lock-time below 10 μ sec and spurs suppression of about -64 dBc at the channel frequency, 2.65 MHz.

II. Design of the Fast-lock Loop Filter

2-1 Passive Fast-lock Loop Filter

Fig. 2 shows a conventional passive fast-lock loop filter. The loop filter in Fig. 2 is located external to the PLL IC, and is constructed using passive chip capacitors and resistors. K_ϕ^* or K_ϕ represent charge pump currents at the fast-lock and normal modes, respectively, and are supplied to the loop filter from the PLL IC. The PLL fast-lock output is connected to one end of resistor R'_2 . The PLL fast-lock output is shorted to the ground when the charge pumper current is K_ϕ^* , and is opened when charge pumper current is K_ϕ . Thus, the resistance of the loop filter change depends on the fast-lock output signal. As a result, the loop filter changes its resistance values depending on the two modes of PLL IC. In the fast-lock mode, the PLL IC supplies charge pump current K_ϕ^* [mA/rad] and the equivalent resistor (R_{eq}) of the loop filter is $R_2 \parallel R'_2$. Since R'_2 is generally small compared to R_2 , the equivalent resistance is approximately equal to R'_2 . Due to small R'_2 , C_2 is charged faster, which results in a faster lock-time. In contrast, the PLL IC supplies a small charge pump current K_ϕ [mA/rad] in the normal mode, and the loop filter resistor value is R_2 . Due to smaller charge pumper current and bigger value of R_2 , C_2 is slowly charged, and spur suppression is consequently improved. The open loop gain for PLL can be expressed as,

$$L(s) = \frac{K_\phi K_v}{Ns^2 C_1} \cdot F(s) = \frac{K_\phi K_v}{Ns^2 C_1} \frac{[1 + sR_{eq}(C_1 \parallel C_2)]}{(1 + sR_{eq}C_2)} \quad (2)$$

where K_v is the tuning sensitivity of VCO. The loop bandwidth from equation (2) is proportional to $\sqrt{K_\phi K_v / (NC_1)}$ [8], [9]. Considering that the variables other than K_ϕ are kept constant, the loop bandwidth is simply proportional to $\sqrt{K_\phi}$.

The resulting change ratio of the loop bandwidth of two modes can be written as,

$$M_i = \sqrt{\frac{K_\phi^*}{K_\phi}} \quad (3)$$

Furthermore, the equivalent resistor (R_{eq}) changes according to the mode change, but the loop bandwidth change given by (3) leaves $F(s)$ unchanged if the change

Fig. 2. Passive fast-lock loop filter.

ratio of R_{eq} is set to $1/M$. The loop bandwidth increases by M but the change in R_{eq} is $1/M$. Thus, $F(s)$ is kept constant for the bandwidth change. Therefore, loop filter shows a scaled behavior although the loop bandwidth changes as in (3).

We select a PLL IC LMX2486 with 16 steps for charge pump current. The minimum charge pump current is $95 \mu\text{A}$ (1X) and the maximum charge pump current is 1.52 mA (16X). The tuning sensitivity of our VCO [10] is measured to be 34.6 MHz/V for the tuning voltage from 0 to 3 V, and the reference frequency is set to 2.65 MHz . Because our VCO supplies $1/4$ frequency output, we measured the $1/4$ frequency out sensitivity, which is found to be 34.6 MHz/V . The synthesized $1/4$ frequency of VCO for the desired X-band frequency was set to 2.69 GHz .

To obtain a lock-time of about $10 \mu\text{sec}$, the loop bandwidth of the fast-lock mode is chosen to be 100 kHz , and the phase margin of the PLL loop filter is set to 45° . According to reference [9], the values of the elements in Fig. 2 are calculated, and the values of the loop filter elements are obtained as $C_1=54 \text{ pF}$, $C_2=262 \text{ pF}$, $R_2=58 \text{ k}\Omega$, and $R'_2=15 \text{ k}\Omega$.

In order to find the effects of the change in the loop filter bandwidth change on lock-time and spur suppression, we separately measured for the two states of the constant loop bandwidth at the 16X and 1X charge pump currents. The first state is when the charge pump current is set to a maximum (16X) in both the fast-lock and normal modes, and this corresponds to constant loop bandwidth of 100 kHz . The second state is that in which the charge pump current is set to a minimum (1X) in both the fast-lock and normal modes. This will yield a 25 kHz loop bandwidth. Thus the fast-lock function is disengaged. However, the lock time and spur suppression when the fast-lock function is engaged can be assessed using two results. The lock time for the 16X charge pumper current provides the best lock time, and

(a) Lock-time (about $10 \mu\text{sec}$)

(b) Spurious performance

Fig. 3. A phase detector constant of 16X (BW=100 kHz).

spur suppression for the 1X offers the best suppression when the fast-lock is engaged. Generally, the combined results of lock time and spur suppression may yield the best result can be obtained.

An Agilent spectrum analyzer 8564E and Agilent digital oscilloscope 54600B were used to measure the lock-time spur response for PLL. The measured lock-time for one-channel shift and the spur response for 16X bandwidth are shown in Fig. 3 and those for 1X are shown in Fig. 4. From Fig. 3(a), the measured lock-time was shown to be about $10 \mu\text{sec}$. The synthesized spectrum in Fig. 3(b) has many fractional spurs that are related to the fractions of the channel frequency. Whereas, the lock-time for 1X is observed to be longer from Fig. 4(a), but the spur response in Fig. 4(b) is shown to be improved.

In summary, the best combined performances when fast-lock is engaged are at a lock-time of 16X in Fig. 3(a) and a spur performance of 1X in Fig. 4(b). Lock-time is estimated to be below $10 \mu\text{sec}$ as desired, however the spur performance is still unsatisfactory, and shows many spur leakages. Additional improvement could be achieved by employing a larger M but is not possible using conventional PLL IC due to the limitation of the

(a) Lock-time (about 60 μ sec)

(b) Spurious performance

Fig. 4. A phase detector constant of 1 X (BW=25 kHz).

charge pumper current change ratio of 16.

From the results in Fig. 3(a) and Fig. 4(b), the loop bandwidth of the fast-lock mode is set to 100 kHz and that of the normal mode is set to 5 kHz. Thus, a bandwidth ratio of 20, which corresponds to a charge pumper current ratio of 400, is required. Considering that the ratio of the charge pumper current is 16 for the PLL IC, an improvement in the order of a factor of 25 should be obtained. This was realized by our active loop filter. Because our loop filter is active, the loop filter noise may degrade the phase noise performance of the synthesized spectrum. Thus, another passive fast-lock loop filter changes from 20 to 5 kHz is designed in order to compare the phase noise at normal modes. The comparison is made possible because the normal mode loop bandwidths of both loop filters are equal.

2-2 Proposed Active Fast-lock Loop Filter

Additional enhancement of the ratio of the charge pump current that is limited by a factor of 16 is desirable for both lock-time and sufficient spur suppression. To overcome the limitation, we propose a novel active fast-lock loop filter shown in Fig. 5. The proposed loop

Fig. 5. Proposed an active fast-lock loop filter.

filter shown in Fig. 5 includes operational amplifiers, switches, and an inverter. The circuit can be partitioned as A, B, and C in terms of their specific operations. The role of part A is to change a charge pump current into a voltage using buffer amplifier A_1 . This voltage is converted into the current by part B, and the current becomes the input of the second amplifier A_2 . Due to the virtual short property, the inverting terminal of A_2 is grounded for AC signal. Thus, the current entering part C is determined by dividing the output voltage of A_1 by the resistor R_F and R_N ($R_N \gg R_F$) in part B. Consequently, the charge pump current is scaled by the resistors in part B.

The loop filter was composed using the impedance in part C. Through the impedance, the scaled current is converted to the proportional voltage and this voltage is used to tune the frequency of the VCO.

In Fig. 5, V_s is the DC supply voltage of PLL IC and the reference voltage is obtained by the voltage division using two identical resistors 10 k Ω , and this reference voltage is also supplied to PLL IC for the reference. Two parallel capacitors denoted by C are bypass capacitors and are used to provide the AC ground, and these values should be set sufficiently large. In part B, we need a series switch in the R_F branch to scale the current. This switch is synchronized to the PLL fast-lock output signal. Switch S_1 is supplied from the PLL fast-lock output is not suitable for direct use as a series switch S_2 because one end is tied to the ground [7]. Therefore, in part B, we constructed the series switch S_2 driven by PLL fast-lock output. In addition, the loop filter in part C is also driven by the fast-lock output at the same time, so that its function is similar to the passive fast-lock loop filter as shown in Fig. 2. Fig. 6 shows a time diagram of switches. From Fig. 6, switches S_2 and S_3 are found to be closed in fast lock mode and open in the normal mode.

Fig. 6. Timing diagram of switches.

The dual supply voltage ± 5 V for operational amplifiers are used. Such supply voltages are chosen because the tuning voltage of VCO ranges from 0 to 3 V. This supplies the VCO tuning voltage without saturation. Operational amplifiers LM6211 from National Semiconductors are used. The DC current dissipation of each operational amplifier is about 1.25 mA, which is selected to be as small as possible. The switches and inverters dissipate small DC current about 0.1 μ A. This is negligible current dissipation considering the total DC current dissipation of our synthesizer about 350 mA.

In the fast-lock mode, a maximum charge current (K_{ϕ}^*) of the PLL IC is supplied to the loop filter input in Fig. 5. Switch S_1 is shorted to the ground in the fast-lock mode. Then, switches S_2 and S_3 are closed by the inverter. Thus, the value of the resistors in part B is $R_F \parallel R_N$. Because R_N is usually much larger than R_F , the value of $R_F \parallel R_N$ is close to about R_F in the fast-lock mode and R_N in the normal mode. In the fast-lock mode, the resulting charge pump current is scaled by the values of R_F and R_{in} . The scaled charge pump current (K_{fast}) in the fast-lock mode is given by

$$K_{fast} = (K_{\phi}^* \times R_{in}) \div R_F. \quad (4)$$

The value of resistor R_{in} is set to 1 k Ω . From equation (4), the charge pump current can be increased by selecting appropriate resistor R_F . This results in an increase in the loop bandwidth.

In the normal mode, the charge pump current is scaled by value of R_N and R_{in} . The scaled charge pump current (K_{normal}) is given by

$$K_{normal} = (K_{\phi} \times R_{in}) \div R_N \quad (5)$$

The value of K_{normal} can be decreased selecting appropriate R_N in (5). This results in loop bandwidth decrease. Consequently, the added charge pumper current change ratio M_e by the proposed circuit alone is given by

$$M_e = \frac{R_N}{R_F \parallel R_N} \cong \frac{R_N}{R_F}. \quad (6)$$

Furthermore, if the charge pump current scaling by PLL IC is included, total charge pump current scaling becomes $16M_e$.

III. Fabrication and Measurement Results

Fig. 7 shows an X-band frequency synthesizer to verify our proposed loop filter. Since the proposed loop filter needs to be compared with other types of loop filters, it is often necessary to replace only the loop filter keeping the rest of circuits preserved. Otherwise, in cases where the loop filter is damaged during the test or comparison, the entire PCB must be repaired. To resolve this problem, we fabricated the loop filter on a separate PCB for ease of replacement, and the loop filter PCB is mounted to the synthesizer PCB using push-on connectors. We selected operational amplifiers LM6211 [12] from National Semiconductor, and inverters 74AHC1G00 [13], and switches 74AHCT1G66 [14] from Philips. The proposed loop filter and X-band frequency synthesizer are fabricated using a four layer PCB process. The top layer is assigned for mounting components and RF part connection. This allows ease of testing. DC bias and control signal lines are placed in the third layer to prevent interference between signals. The second and fourth layers are assigned for the grounds.

To supply the control signal to the PLL IC using the driving program, a 9-pin connector is mounted. A single voltage of 10 V DC is supplied from the DC power supply. Two regulators 3.3 and 5 V are used for the PLL IC and for biasing the VCO, and are distributed to other active devices requiring a DC supply.

For a faster lock-time, the loop bandwidth of the proposed loop filter should be set to 100 kHz in the fast-lock mode and 5 kHz in the normal mode as previously explained. The value of resistor R_{in} is set to 1 k Ω . The values of resistors R_N and R_F were set to provide $M_e=25$, and were chosen as 25 k Ω and 1 k Ω , respectively. The values of R_F and R_N provide the charge pump current approximately equal in fast-lock mode and the decreased one by about 1/25 times in normal mode. Thus, the normal mode is around 3.8 μ A. With the PLL IC scaling included, the charge pumper current change ratio for fast-lock to normal modes is about 400. The corresponding loop bandwidth change is then 20. The element values in the proposed loop filter are similarly computed as in the passive loop filter. According to [11], the component values are computed to be $C_1=54$ pF, $C_2=262$ pF, $R_2=300$ k Ω , and $R'_2=15$ k Ω with a 45° phase margin.

Fig. 7. Fabricated X-band frequency synthesizer.

Fig. 8. Lock-time of the X-band frequency synthesizer. Fast-lock mode loop bandwidth=10 kHz, and normal mode loop bandwidth=5 kHz.

It can be seen from Fig. 8 that the lock-time is below 10 μ sec. The measured waveform of the lock-time shows some overshoot. This result is considered to be due to the parasitic elements. It is also clear from Fig. 9 that the center frequency is about 10 GHz and the spurs are suppressed to about -64 dBc.

Fig. 10 shows a comparison of the synthesized signals for passive and active fast-lock loop filters. The passive fast-lock filter is set to a loop bandwidth change from 20 to 5 kHz. For comparison, the normal mode bandwidth is set equal to that of the active fast-lock filter. The element values are $C_1=1,500$ pF, $C_2=6,600$ pF, $R_2=12$ k Ω , and $R'_2=3.6$ k Ω with a 45° phase margin. When locked, the spectra are found to be almost equal. Also for comparison, the spectrum of 100 kHz loop bandwidth is shown. Due to a bandwidth improvement of 20 (100/5), the phase noise of the loop bandwidth 5 kHz shows an improvement of about 40 dB. However, near

Fig. 9. Spectrum of X-band synthesized signal (BW=5 kHz). A 9-dB attenuator was added to the VCO output.

Fig. 10. Comparison of spectra of X-band synthesized signals for passive and active fast-lock loop filters. A 9-dB attenuator was added to the VCO output.

carrier phase noise is not clearly shown. Thus we measured phase noise again for active and passive fast-lock filters using a phase noise measurement utility installed in a spectrum analyzer.

Fig. 11 shows the measured spectra. Note that the spectra are for normal modes. The spectra show a flat phase noise up to about a 5 kHz offset frequency, which is loop bandwidth both for passive and active fast-lock loop filters. Two phase noises coincide closely outside

Fig. 11. Measured phase noise of X-band synthesized signals for passive and active fast-lock loop filter (BW= 5 kHz).

the loop bandwidth. The phase noise of passive loop filter shows a low value about 10 dB. The reason for this is believed to be the added noise from operational amplifiers. This may be the cost associated with using operational amplifiers in the loop filter, which aim to improve lock time. The in-band phase noise is degraded by 10 dB. When such degradation is not tolerable, our loop filter cannot be applied.

The result of this paper is compared with some commercial X-band frequency synthesizers. In Table 1, the spur suppression of this work is shown to be to those of other frequency synthesizers. However, the performance index is much smaller than for other frequency synthesizers. The performance index of the lock-time is determined by multiplying the frequency step and the lock-time. In case that frequency step is high, we can select

Table 1. Comparison of this work with commercial products.

Items	KOSPACE [15]	TRAK Corp. [16]	This work
Frequency range	X-band	X-band	X-band
Frequency step	27 MHz	5 MHz	2.65 MHz
Lock-time	3 msec	1 msec	10 μ sec
Spurious suppression	-70 dBc	-60 dBc	-64 dBc
Performance index	81000	5000	24

a wider loop bandwidth and faster lock-time results. When lock-time is fast, despite small frequency step, the lock-time performance of the frequency synthesizer is assessed to be a better one. In order words, a small performance index indicates a better performance. Based upon such performance index criteria, our proposed frequency synthesizer is proven to be an excellent one.

IV. Conclusion

In this paper, a fast-lock technique for PLL to overcome the trade-off between lock-time and spur suppression is presented. In order to overcome the limitation of the charge pumper current ratio in conventional PLL ICs, we propose a novel active fast-lock loop filter. Due to such enhancement, we can simultaneously achieve a faster lock-time and high spur suppression. To verify its performance, the proposed loop filter was applied to an X-band frequency synthesizer. The fabricated X-band synthesizer shows an excellent performance with a lock-time below 10 μ sec and a reference spur of around -64 dBc at 2.65 MHz.

This work was supported by National Research Foundation of Korea Grant funded by the Korean Government (KRF-2010-0016934)

References

- [1] U. L. Rohde, *Microwave and Wireless Synthesizers Theory and Design*, Wiley, pp. 1-4, 1997.
- [2] C. S. Vaucher, "An adaptive PLL tuning system architecture combining high spectral purity and fast settling time," *IEEE J. Solid State Circuits*, vol. 35, no. 4, pp. 490-502, Apr. 2000.
- [3] W. H. Chiu, Y. H. Huang, and T. H. Lin, "A dynamic phase error compensation technique for fast-locking phase-locked loop," *IEEE J. Solid State Circuits*, vol. 45, no. 6, pp. 1137-1148, Jun. 2010.
- [4] K. H. Woo, Y. Liu, E. Nam, and D. H. Ham, "Fast-lock hybrid PLL combining fractional-N and integer-N modes of differing bandwidths," *IEEE J. Solid State Circuits*, vol. 43, no. 2, pp. 379-389, Feb. 2008.
- [5] X. F. Kuang, N. J. Wu, "A fast-settling PLL frequency synthesizer with direct frequency presetting," in *IEEE ISSCC Dig. Tech. Papers*, pp. 741-742, Feb. 2006.
- [6] S. Shin, K. Lee, and S. -M. Kang, "4.2 mW CMOS frequency synthesizer for 2.4 GHz ZigBee application with fast settling time performance," in *Micro-wave Symp. Dig.*, pp. 411-414, Jun. 2006.

- [7] LMX2486, 1~4.5 GHz High Performance Delta-sigma Low Power Dual PLLatinum Frequency Synthesizers with 3 GHz integer PLL, National, Available: <http://www.national.com>
- [8] D. Barberjee, *PLL Performance, Simulation, and Design*, 4th Ed., 2006.
- [9] National Semiconductor, *A Fast Locking Scheme for PLL Synthesizer*, AN-1000, 1995.
- [10] HMC514LP5, MMIC VCO w/Half frequency output & divide-by-4, 11.17~12.02 GHz, Hittite, Available: <http://www.hittite.com>
- [11] National Semiconductor, *PLL Performance, Simulation, and Design*, 2nd Ed., 2001.
- [12] LM6211, Low Noise, RRO Operational Amplifier with CMOS Input and 24V Operation, National, Available: <http://www.national.com/>
- [13] 74AHC1G00, *Inverter*, Philips, Available: <http://www.semiconductors.philips.com/>
- [14] 74AHCT1G66, Bilateral switch, philips, Available: <http://www.semiconductors.philips.com/>
- [15] MIL-STD-810, X-band synthesizer, KOSPACE Available: <http://www.kospace.com>
- [16] X-BAND SYNTHESIZER, TRAK. Microwave Corporation, Available: <http://www.trak.com>

Yun-Seong Heo

His research interests are microwave active circuit and system design.

was born in Seoul, Korea, in 1987. He received B.S. degrees in radio science and engineering from Chungnam National University, Daejeon, Korea, in 2006 and 2010, respectively and is currently working toward M.S. degree in radio science and engineering at Chungnam National University. His research interests are microwave active circuit and system design.

Hae-Chang Jeong

search interests are in the design of hybrid and monolithic microwave circuits and systems.

was born in Cheonan, Korea, in 1984. He received the B.S. and M.S. degrees in radio science and engineering from Chungnam National University, Daejeon, Korea, in 2008 and 2010, respectively and is currently working toward the Ph.D. degree in radio science and engineering at Chungnam National University. His research interests are in the design of hybrid and monolithic microwave circuits and systems.

Hyun-Seok Oh

research interests are in the design of hybrid and monolithic microwave circuits and systems.

was born in Seoul, Korea, in 1979. He received the B.S. and M.S. degrees in radio science and engineering from Chungnam National University, Daejeon, Korea, in 2003 and 2007, respectively and is currently working toward the Ph.D. degree in radio science and engineering at Chungnam National University. His research interests are in the design of hybrid and monolithic microwave circuits and systems.

Kyung-Wan Yeom

to 1991, he was with LG Precision, as a Principal Engineer. He worked with the MIC team as a team leader and was involved subsequently in military electronics division for electronic warfare (EW) equipments. From 1991 to 1995, he was with LTI, where he was involved with power amplifier modules for analog cellular phones. In 1995, he joined Chungnam National University as an Assistant Professor. He is currently a Professor with the Department of Radio Science and Engineering, Chungnam National University, Daejeon, Korea. He was the Editor-in-Chief of the Korean Institute of Electromagnetic Engineering and Science (KIEES) from 2004 to 2006. His research interests are in the design of hybrid and monolithic microwave circuits and microwave systems. Prof. Yeom has been a member of KIEES since 1995. He was the recipient of the IR-52 Jang Youn-Sil Prize from MOST of Korea for his research on cell phone power amplifiers at 1994. He was also the recipient of the Academic Award from KIEES for "Design and fabrication of a novel 60 GHz GaAs pHEMT resistive double balanced star MMIC mixer" in 2004.

was born in Seoul, Korea, in 1957. He received the B.S. degree in electronics from Seoul National University, Seoul, Korea, in 1980, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1982 and 1988, respectively. From 1985