Integrated Circuit Design Based on Carbon Nanotube Field Effect Transistor

Yong-Bin Kim[†]

Department of Electrical and Computer Engineering, Northeastern University, Boston, MA, USA

As complementary metal-oxide semiconductor (CMOS) continues to scale down deeper into the nanoscale, various device non-idealities cause the I-V characteristics to be substantially different from well-tempered metal-oxide semiconductor field-effect transistors (MOSFETs). The last few years witnessed a dramatic increase in nanotechnology research, especially the nanoelectronics. These technologies vary in their maturity. Carbon nanotubes (CNTs) are at the forefront of these new materials because of the unique mechanical and electronic properties. CNTFET is the most promising technology to extend or complement traditional silicon technology due to three reasons: first, the operation principle and the device structure are similar to CMOS devices and it is possible to reuse the established CMOS design infrastructure. Second, it is also possible to reuse CMOS fabrication process. And the most important reason is that CNTFET has the best experimentally demonstrated device current carrying ability to date. This paper discusses and reviews the feasibility of the CNTFET's application at this point of time in integrated circuits design by investigating different types of circuit blocks considering the advantages that the CNTFETs offer.

Keywords: Nano-technology, Complementary metaloxide semiconductorscaling, Integrated circuit, Carbon nanotube, Carbon nanotube field effect transistor, Very largescale integration, Nano-electronics

1. INTRODUCTION

Complementary metal-oxide semiconductor (CMOS) technology scaling has been enabling higher integration capacity in very largescale integration (VLSI) designs. Over the last few years, devices at 32 nm have been manufactured and the deep sub-micron/nano range of below 10 nm is foreseen to be reached in the near future as technology continues to scale down. In the 32 nm technology era, the leakage current has substantially increased, and the sensitivity to process variations in manufacturing is considered to be almost unavoidable. Due to the lower power supply and the smaller node capacitance, the amount of charge stored on a circuit node is becoming increasingly smaller, thus making circuits more susceptible to spurious voltage variations caused by externally induced phenomena such as cosmic ray neutrons

and α -particles [1]. Therefore, robust CMOS circuits design techniques is becoming crucial in the nanoscale era.

Technology boosters such as strain have helped the continuation of CMOS historic performance trend up to 45 nm node. As device physical gate length is reduced to below 25 nm at/beyond 65 nm technology node, various leakage currents and device parameter variation become the most important considerations for device optimization. In fact, it can be argued that reduction of gate length below 25 nm may not offer the same advantage as short-gate devices had provided historically in terms of power and performance at the system level [2]. The major detractors are: the lack of a thin equivalent gate oxide (with low leakage current) for effective short channel effect control, the increasing contribution of the fringing parasitic capacitance to the total gate capacitance, and the rising contribution of the source/drain resistance to the total device on-resistance [3]. Moreover, various device non-idealities cause the I-V characteristics to be substantially different from well-tempered metal-oxide semiconductor field-effect transistors (MOSFETs). It becomes more difficult to further improve device/circuit performance by reducing the physical gate length.

[†] Author to whom all correspondence should be addressed:
E-mail: ybk@ece.neu.edu

Copyright ©2011 KIEEME. All rights reserved.

This is an open-access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (<http://creativecommons.org/licenses/by-nc/3.0>) which permits unrestricted noncommercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

Fig. 1. Unrolled graphite sheet.

Therefore, new materials and devices have been investigated to replace silicon in nanoscaled transistors from the year 2015 and beyond. As one of the promising new devices, carbon nanotube FETs (CNTFETs) avoid most of the fundamental limitations for traditional silicon devices, due to their unique one-dimensional band-structure that suppresses backscattering and makes near-ballistic operation realistic possibility [4-7]. A single-walled CNT (SWCNT) can be visualized as a sheet of graphite, which is rolled up and joined together along a roll-up vector as shown in Fig. 1.

Depending on the chiral angle (roll-up vector or chirality vector), the CNT can be either semiconducting or metallic. By considering the indices (n, m) shown in Fig. 1, the nanotube is metallic if $n = m$ or $n - m = 3i$ where i is an integer. Otherwise, the tube is semiconducting. CNTFETs are the FETs that make use of semiconducting CNTs as channel material between two metal electrodes that act as source and drain contacts. The operation principle of CNTFET is similar to that of traditional silicon devices. As shown in Fig. 2, this three (or four) terminal device consists of a semiconducting nanotube, acting as conducting channel, bridging the source and drain contacts. The device is turned on or off electrostatically via the gate. Despite several serious technological barriers, CNTFETs with their small feature size and high-current capability show a potential for performance improvement compared with CMOS transistors.

The CV/I performance of an intrinsic CNTFET is 13 times better than the CV/I performance of a bulk n-type MOSFET because the CNTFETs effective gate capacitance of one CNT per gate is about 4% compared to bulk CMOS and the driving current ability of each CNT is about 50% of a bulk n-type MOSFET with minimum gate width (48 nm) at a 32 nm node (due to the ballistic transport nature of a CNT). Moreover due to the similar behavior and the current driving capability of a pFET compared to those of an nFET, the performance improvement of a pFET over a PMOS is better than the one of a nFET over a NMOS. Even though a CNTFET has a leakage current in the off-state, this leakage current is controlled by the full band gap of the CNTs and the band to band tunneling; this is less than for a MOSFET [8,9].

The expected (optimistic) performance advantage of a CNTFET (as described previously) is unlikely to be achievable in a real device and will be significantly degraded for the CV/I (6 times for a nFET and 14 times for a pFET) due to device/circuit non-ideal conditions. These non-ideal conditions include the series resistance of the doped source/drain region, the Schottky barrier (SB) resistance at the metal/CNT interface, the gate outer-fringe capacitance and the interconnect wiring capacitance. However, the need for low power consumption and high operating frequency has resulted in geometry and supply scaling with a significant increase in operating temperature for a device. With these scaling features, the effects of systematic and random variations in process, supply voltage, and temperature (PVT) may cause an

Fig. 2. Cross section view of a CNTFET. CNTFET: carbon nanotube field-effect transistor.

inconsistent delay and increase in leakage to appear even in low power circuits, thus becoming one of the major challenges in nanoscale devices. Therefore, to measure the actual performance of a CNTFET compared to a MOSFET, it is necessary to compare performance at a circuit level under different conditions. In this paper, logic gates and benchmark circuits are designed at 32 nm for both CNTFET and CMOS technologies to assess the advantages of combinational logic gates using CNTFET; delay, power, power delay product (PDP), leakage current and frequency response are simulated and compared [8-10].

After the performance assessment of CNTFET based combinational logic gates, ternary logic gates is investigated as a part of combinational gate design to take advantage of the CNTFET technology. In a CNTFET, the threshold voltage of the transistor is determined by the diameter of the CNT. Therefore, a multi-threshold design can be accomplished by employing CNTs with different diameters (and, therefore, chirality) in the CNTFETs. A resistive-load CNTFET-based ternary logic design has been proposed in [11]. However, in this configuration, large OFF-chip resistors (of at least 100 M Ω values) are needed due to the current requirement of the CNTFETs. The design technique proposed in this paper relies on [12] and eliminates the large resistors by employing active load with P-type CNTFETs in the ternary logic gates. Ternary logic (or three-valued logic) has attracted considerable interest due to its potential advantages over binary logic for designing digital systems. For example, it is possible for ternary logic to achieve simplicity and energy efficiency in digital design since the logic reduces the complexity of interconnects and chip area. The multivalued logic design based on multi-threshold CNTFETs is assessed and compared with existing multivalued logic designs based on CNTFETs in this paper.

Another type of digital circuits required to build a digital system is sequential element such as latch or flip-flop to store data for pipeline structure. CMOS storage elements, such as CMOS memories and latches, usually include a data storage circuit or circuit element, which is capable to hold one bit of binary information. The storage cell also includes a data access device, for example, a pass gate transistor for static random access memory (SRAM) cell, or a transmission gate for latch. The data access device allows or disallows data read or write from and to the storage circuit depending on the state of the control signal on the control node of the access device. Additional circuit elements may be used to improve environmental tolerance and to accommodate a variety of functions in a single memory cell [13]. As device density increases, a larger fraction of chip area is devoted to the on-chip memory modules, because on-chip memory helps improve the micro-architectural performance of a microprocessor. Several of the latest processor designs showed that around 50% of the chip area was occupied by caches [14]. Meanwhile, latches and D flip-flops, which are the basic building blocks of the sequential circuits, also take a large area of the latest chips. This paper studies on the analysis and design of robust storage elements in both 32 nm CMOS technology and novel CNTFETs for comparison

Fig. 3. Voltage transfer characteristic for 32 nm metal-oxide semiconductor field-effect transistor (MOSFET) and carbon nanotube FET (CNTFET) inverters at 0.9 V supply voltage.

and feasibility study. In this paper, the feasibility is studied for the robust design of two major storage elements (latch and memory cell) in modern integrated circuits.

Section 2 discusses and assesses the CNTFET based combinational logic gates in comparison with CMOS nanoscale combinational logic gates, and ternary logic gates are proposed and its performance is studied in Section 3. Section 4 presents the memory elements design and their performance in comparison with their nanoscale CMOS counterpart, followed by conclusion in Section 5.

2. CNTFET BASED LOGIC GATE PERFORMANCE ANALYSIS

To measure the actual performance of a CNTFET compared to a MOSFET, it is necessary to compare performance at a circuit level under PVT variations. In this paper, logic gates and benchmark circuits are designed at 32 nm for both CNTFET and CMOS technologies; delay, power, PDP, leakage current and frequency response are simulated and compared [8-10].

2.1 Ratio between PMOS and NMOS

For comparing the performance of CNTFETs with MOSFETs at circuit level, the inverter as a fundamental logic gate is considered first; the inverter is designed with minimal width and a number of tubes in 32 nm technology. For Si CMOS, a PMOS/NMOS ratio between 2 and 3 is used for compensating the difference in mobility between PMOS and NMOS. In this paper, a 3 to 1 (PMOS:NMOS) ratio is used when designing the inverter because the voltage transfer characteristic (VTC) of the MOSFET inverter shows a more symmetrical shape in the center of the logic threshold voltage ($V_{DD}/2$) for a ratio of 3 in 32 nm as shown in Fig. 3.

However, for the CNTFET case, a 1 to 1 (pFET:nFET) ratio is used because the nFET and the pFET have almost the same current driving capability with same transistor geometry [8]. Figure 3 shows that the VTC of the CNTFET also has a symmetrical shape at a 1 to 1 (pFET:nFET) ratio. Even though the current in a CNT is smaller than the minimum sized MOSFET (at 32 nm technology), a CNTFET has a steeper curve in the transition region due to the higher gain. This contributes to a 22.5% improvement in noise margin (NM), and this progressed performance is preserved under a decrease in power supply voltage as shown in Fig. 4. In this paper, the ratio value used for the inverter is also uti-

Fig. 4. Voltage transfer characteristic of 32 nm carbon nanotube field-effect transistor (CNTFET) and metal-oxide semiconductor FET (MOSFET) inverters at different power supplies.

Table 1. Delay, power, and PDP for 32 nm MOSFET and 32 nm CNTFET logic gates.

		Delay (sec)	Power (watt)	PDP (joule)
MOSFET	Inverter	1.77E-11	1.39E-06	2.46E-17
	NAND2	2.26E-11	1.96E-06	4.41E-17
	NAND3	2.99E-11	2.77E-06	8.29E-17
	NOR2	3.97E-11	2.58E-06	1.02E-16
	NOR3	6.97E-11	4.04E-06	2.82E-16
CNTFET	Inverter	2.42E-12	1.11E-07	2.69E-19
	NAND2	3.49E-12	1.89E-07	7.41E-19
	NAND3	5.06E-12	2.90E-07	1.47E-18
	NOR2	3.50E-12	1.85E-07	6.48E-19
	NOR3	5.08E-12	2.73E-07	1.39E-18

PDP: power delay product, MOSFET: metal-oxide semiconductor field-effect transistor, CNTFET: carbon nanotube field-effect transistor.

lized when designing more complex logic gates and benchmark circuits and used to determine the width and number of tubes of the CNTFET. To determine the PMOS/NMOS ratio for CMOS, the transistor width (W) of a MOSFET is modified; however in a CNTFET, the number of CNTs is changed because a CNTFET uses CNTs for the conducting channel between the source and drain. Therefore, when the width of the CNTFET is changed, by implication the number of tube is also changed.

2.2 Logic gates performance analysis

In this section, different metrics are utilized to compare CNTFET and CMOS logic gates at 32 nm features size. The design performance metrics used to compare the two different technology based logic gates are PDP, leakage power, PVT variation, and frequency response.

2.2.1 Power delay product

Due to the increased demand for high-speed, high-throughput computation, and complex functionality in mobile environments, reduction of delay and power consumption is very challenging. MOSFET and CNTFET can be compared using the PDP as metric. Table 1 shows the delay, power, and PDP of logic gates in 32 nm MOSFET and 32 nm CNTFET technologies; the PDP of the 32 nm MOSFET is about 100 times higher than that of the 32 nm CNTFET.

Fig. 5. Maximum and minimum leakage power for 32 nm metal-oxide semiconductor field-effect transistor (MOSFET) and carbon nanotube FET (CNTFET) logic gates.

2.2.2 Leakage power

As process dimensions shrink further into the nanometer ranges, traditional methods for dynamic power reduction are becoming less effective due to the increased impact of static power [15]. In general, leakage power is different depending on the applied input vector. Figure 5 shows the maximum and minimum leakage power for 32 nm MOSFET and CNTFET based logic gates. The maximum leakage power of the MOSFET-based gates is 75 times larger than for CNTFET gates. The minimum leakage power of the MOSFET is about three times larger than for CNTFET. Figure 5 also shows that the maximum leakage power shows a similar trend for both CNTFET and MOSFET-based gates, while the minimum leakage power shows somewhat different trends, because the stack effect is reduced in CNTFET circuits.

2.2.3 Frequency response

For establishing the frequency response, AC simulation has been performed for both the MOSFET and CNTFET inverters. The results are given in Fig. 6, where the CNTFET inverter shows nearly 3dB more voltage gain and 3 times higher 3dB frequency (f_{3dB}) than the MOSFET inverter, thus confirming its superiority in terms of this metric.

2.2.4 PVT variations

With technology scaling, the effects of systematic and random

Fig. 6. Frequency response for 32 nm metal-oxide semiconductor field-effect transistor (MOSFET) and carbon nanotube FET (CNTFET) inverters.

Fig. 7. I_{DS} (drain-to-source current) vs. V_{GS} (gate-to-source voltage) with 10% change of carbon nanotube (CNT) diameter (chirality) for the 32 nm CNTfield-effect transistor (FET).

variations in PVT have led to inconsistent delay and leakage in low power circuits, thus becoming a major obstacle for device scaling. Significant levels of process variations affect technology scaling beyond 90 nm, and they are changing the design environment from a deterministic to a probabilistic one. Moreover, the requirement of low power relies on supply voltage scaling, making voltage variations a significant challenge. The quest for increase in higher operating frequencies has resulted in significantly high junction temperature and within-die temperature variation [10,16]. Therefore, the possible performance degradation due to PVT variations has become a major criterion in assessing the performance of a new technology.

2.2.4.1 Process variation

When investigating physical process variations, among them channel length and widths are considered for CMOS MOSFET.

However, CMOS and CNTFET have different characteristics. The current change in a MOSFET is about $\pm 30\%$ ($\pm 13\%$) for a $\pm 10\%$ change in length (width) at a gate voltage of 0.9 V while the current change in a CNTFET is below $\pm 0.5\%$. However when the diameter of the CNTFET is changed by $\pm 10\%$, the current change in a CNTFET is about $\pm 17\%$ as shown in Fig. 7. Therefore for a CNTFET, the diameter variation is more important because a CNTFET is more sensitive to diameter variation than

Fig. 8. Power delay product (PDP) of 32 nm carbon nanotube field-effect transistor (CNTFET) logic gates vs. diameter (chirality) of CNT.

Fig. 9. Maximum leakage power of the 32 nm carbon nanotube field-effect transistor (CNTFET) logic gates vs. diameter (chirality) of CNT.

length and width variations. Based on this observation, the PDP and leakage of a CNTFET are computed and shown in Figs. 8 and 9, respectively. When the diameter of a CNTFET is changed, then the PDP changes too. Figure 9 shows that the maximum leakage power increases when the diameter is increased. Also note that the threshold voltage and diameter of a CNTFET are determined based on the chirality of the CNTs used in this type of transistor.

2.2.4.2 Voltage variation

The reduction in power consumption due to voltage scaling is also confronted with the increased sensitivity to voltage variations; this is a major concern to assess the performance of a new technology such as CNTFETs. Figures 10 and 11 show the PDP for 32 nm MOSFET and CNTFET logic gates, respectively when the supply voltage is decreased until the gate stops functioning. These figures show that the inverter and the other logic gates op-

Fig. 10. Power delay product (PDP) of 32 nm metal-oxide semiconductor field-effect transistor (MOSFET) logic gates vs. supply voltage.

Fig. 11. Power delay product (PDP) of 32 nm carbon nanotube field-effect transistor (CNTFET) logic gates vs. supply voltage.

Fig. 12. Power delay product (PDP) of 32 nm metal-oxide semiconductor field-effect transistor (MOSFET) logic gates vs. temperature.

erate until the supply voltage decreases to 0.5 V and 0.6 V, respectively. Even though the PDP is changed depending on the supply voltage, this change is more or less the same as the change in PDP for the MOSFET logic gates; hence, the overall PDP of the CNTFET-based gates is significantly lower than for the MOSFET-based gates.

Fig. 13. Power delay product (PDP) of 32 nm carbon nanotube field-effect transistor (CNTFET) logic gates vs. temperature.

2.2.4.3 Temperature variation

As the circuit speed increases, a larger power consumption is often encountered, thus resulting in more heat at chip level. Circuits with an excessive power dissipation are more susceptible to run-time failures and account for serious reliability problems [10,16]. Figures 12 and 13 show that the PDP of the MOSFET gates increases with temperature; however, the PDP of the CNTFET logic gates is constant. Moreover, the maximum leakage power of the MOSFET gates increases linearly with temperature, while for the CNTFET-based gates this increase is exponential.

Few combinational circuits (such as a 4 stage inverter chain, a 2:4 decoder, a 4:16 decoder, the ISCAS-85 Benchmark Circuit C17, a 1-bit full adder, a 3-bit Ripple Carry Adder, and the ISCAS-85 Benchmark Circuit 74182) have also been evaluated. The average delay and power consumption of the 32 nm MOSFET circuits is about 10 times and 100 times higher than those of the 32 nm CNTFET circuits respectively; these results confirm the findings found in the previous sub-sections for the CNTFET and MOSFET logic gates. Moreover, it shows that indeed CNTFET based design offer significant improvements over MOSFET-based designs.

3. TERNARY LOGIC GATE DESIGN USING CNTFET

Digital computation has been performed on two-valued logic, i.e., there are only two possible values (0 or 1, true or false) in the Boolean space. Multiple-valued logic (MVL) replaces the classical Boolean characterization of variables with either finitely or infinitely many values such as ternary logic [17] or fuzzy logic [18]. Ternary logic (or three-valued logic) has attracted considerable interest due to its potential advantages over binary logic for designing digital systems. For example, it is possible for ternary logic to achieve simplicity and energy efficiency in digital design since the logic reduces the complexity of interconnects and chip area [19]. Furthermore, serial and serial-parallel arithmetic operations can be carried out faster if the ternary logic is employed. Extensive research on design and implementation of ternary logic using CMOS can be found in the technical literature [19,20]. Chip area and power dissipation can be reduced by more than 50% using an efficient MVL implementation for a signed 32-bits multiplier compared to its fastest binary counterpart [11]. MVL modules have been inserted into binary logic ICs to enhance the performance of CMOS technologies [21].

There are two kinds of MVL circuits based on MOS technology,

Table 2. Logic symbols.

Voltage level	Logic value
0	0
$1/2 V_{dd}$	1
V_{dd}	2

Table 3. Truth table of STI, PTI, and NTI.

Input X	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

STI: standard ternary inverter, PTI: positive ternary inverter, NTI: negative ternary inverter.

namely the current-mode MVL circuits and the voltage-mode MVL circuits. Voltage-mode MVL circuits have been achieved in multi-threshold CMOS design [22]. In a CNTFET, The threshold voltage of the transistor is determined by the diameter of the CNT. Therefore, a multi-threshold design can be accomplished by employing CNTs with different diameters (and, therefore, chirality) in the CNTFETs. A resistive-load CNTFET-based ternary logic design has been proposed in [11]. However, in this configuration, large OFF-chip resistors (of at least 100 MΩ values) are needed due to the current requirement of the CNTFETs. The design technique proposed in [23] relies on [12] and eliminates the large resistors by employing active load with P-type CNTFETs in the ternary logic gates. In this paper, the multivalued logic design based on multi-threshold CNTFETs is assessed and compared with existing multivalued logic designs based on CNTFETs.

Ternary logic functions are defined as those functions having significance if a third value is introduced to the binary logic. In this paper, 0, 1, and 2 denote the ternary values to represent false, undefined, and true, respectively. Any n variable $\{X_1, \dots, X_n\}$ ternary function $f(X)$ is defined as a logic function mapping $\{0,1,2\}^n$ to $\{0, 1, 2\}$, where $X = \{X_1, \dots, X_n\}$. The basic operations of ternary logic can be defined as follows, where $-$ denotes the arithmetic subtraction, the operations $+$, $\bullet$, and $\overline{}$ are referred to as the OR, AND, and NOT in ternary logic, respectively. The fundamental gates in the design of digital systems are the inverter, the NOR gate, and the NAND gate. The assumed logic symbols are shown in Table 2. The ternary gates are designed according to the convention defined by Eq. (1).

$$X_i, X_j = \{0,1,2\} [13]:$$

$$X_i + X_j = \max\{X_i, X_j\}, X_i \bullet X_j = \min\{X_i, X_j\}, \overline{X_i} = 2 - X_i \quad (1)$$

3.1 Ternary inverter

A general ternary inverter is an operator (gate) with one input x , and three outputs (denoted by y_0 , y_1 , and y_2) such that

$$\begin{aligned} y_0 &= C_0(x) = \begin{cases} 2, & \text{if } x = 0 \\ 0, & \text{if } x \neq 0 \end{cases} \\ y_1 &= C_1(x) = \overline{x} = 2 - x \\ y_2 &= C_2(x) = \begin{cases} 2, & \text{if } x \neq 2 \\ 0, & \text{if } x = 2 \end{cases} \end{aligned} \quad (2)$$

Therefore, the implementation of ternary inverter requires three inverters, and they are a negative ternary inverter (NTI), a

Table 4. Truth table of NAND and NOR gates.

Input X_1	Input X_2	Y_{NAND}	Y_{NOR}
0	0	2	2
1	0	2	1
2	0	2	0
0	1	2	1
1	1	1	1
2	1	1	0
0	2	2	0
1	2	1	0
2	2	0	0

standard ternary inverter (STI), and a positive ternary inverter (PTI), if y_o , y_1 , and y_2 in (2) are the outputs [19]. The truth table of the three ternary inverters is shown in Table 3.

3.2 Ternary NOR and NAND gates

The ternary NAND and NOR are two multiple entry operators used in ternary logic. The functions of the two-entry ternary NAND and NOR gates are defined by the following two equations, respectively [20]:

$$Y_{\text{NAND}} = \overline{\min\{X_1, X_2\}} \quad (3)$$

$$Y_{\text{NOR}} = \overline{\max\{X_1, X_2\}} \quad (4)$$

The truth table for the ternary NAND and NOR gates is shown in Table 4.

3.3 CNTFET threshold voltage

CNTFETs utilize semiconducting SWCNTs to assemble electronic devices [24]. A SWCNT consists of one cylinder only, and the simple manufacturing process of this device makes it very promising for alternative to today's MOSFET. A SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (n, m) . A simple method to determine if a CNT is metallic or semiconducting is to consider its indexes (n, m) : the nanotube is metallic if $n = m$ or $n - m = 3i$, where i is an integer. Otherwise, the tube is semiconducting. The diameter of the CNT can be calculated based on the following [3,8,25]:

$$D_{\text{CNT}} = \frac{\sqrt{3}a_0}{\pi} \sqrt{n^2 + m^2 + nm} \quad (5)$$

where $a_0 = 0.142$ nm is the interatomic distance between each carbon atom and its neighbor. The I-V characteristics of the CNTFET are similar to MOSFET's. The threshold voltage is defined as the voltage required to turn ON transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap that is an inverse function of the diameter [3,8,25], i.e.

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV\pi}{eD_{\text{CNT}}} \quad (6)$$

where $a = 2.49$ angstrom is carbon to carbon atom distance, and $V\pi = 3.033$ eV is the carbon π - π bond energy in the tightbonding

Fig. 14. Carbon nanotube field-effect transistor-based standard ternary inverter design.

Fig. 15. Voltage transfer characteristic of standard ternary inverter in Fig. 14.

model, e is the unit electron charge, and D_{CNT} is the CNT diameter. As D_{CNT} of a $(19, 0)$ CNT is 1.487 nm, the threshold voltage of a CNTFET using $(19, 0)$ CNTs as channels is 0.293 V from Eq. (6). As the chirality vector changes, the threshold voltage of the CNTFET will also change. Assume that m in the chirality vector is always zero, and then the ratio of the threshold voltages of two CNTFETs with different chirality vectors is given as:

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{\text{CNT2}}}{D_{\text{CNT1}}} = \frac{n_2}{n_1} \quad (7)$$

Equation (7) shows that the threshold voltage of a CNTFET is inversely proportional to the chirality vector of the CNT. For example, the threshold voltage of a CNTFET using $(13, 0)$ CNTs is 0.428 V, compared to a $(19, 0)$ CNTFET with a threshold voltage of 0.293 V.

3.4 CNTFET based ternary inverter design

A CNTFET-based ternary logic design has been initially pro-

Fig. 16. Schematic diagram of (a) negative ternary inverter and (b) positive ternary inverter.

Fig. 17. Symbols of (a) negative ternary inverter, (b) standard ternary inverter, and (c) positive ternary inverter.

posed in [11]. It employs dual-diameter CNTFETs and resistors. However, two large resistors (usually 100 M Ω or greater) are required to implement the design, but their values are too large to be integrated into CNTFET technology. Lin et al. [23] proposed CNTFET-based STI design; the STI in Fig. 14 consists of six CNTFETs. The chiralities of the CNTs used in T1, T2, and T3 are (19, 0), (10, 0), and (13, 0), respectively. From Eq. (5), the diameters of T1, T2, and T3 are 1.487, 0.783, and 1.018 nm, respectively. Therefore, the threshold voltages of T1, T2, and T3 are 0.289, 0.559, and 0.428 V, respectively from Eq. (6). The threshold voltages of T5, T6, and T4 are -0.289, -0.559, and -0.428 V, respectively. When the input voltage changes from low to high at the power supply voltage of 0.9 V, initially, the input voltage is lower than 300 mV. This makes both T5 and T6 turn ON, both T1 and T2 turn OFF, and the output voltage becomes 0.9 V, i.e. logic 2. As the input voltage increases beyond 300 mV, T6 is OFF and T5 is still ON. Meanwhile, T1 is ON and T2 is OFF. The diode connected CNTFETs T4 and T3 produce a voltage drop of 0.45 V from node n2 to the output, and from the output to n1 due to the threshold voltages of T4 and T3. Therefore, the output voltage becomes 0.45 V, i.e., half of the power supply voltage. As shown in Table 2, half V_{dd} represents logic 1. Once the input voltage exceeds 0.6 V, both T5 and T6 are OFF, and T2 is ON to pull the output voltage down to zero. The input voltage transition from high to low transition is similar to the low to high transition.

Simulation on these STIs has been performed by HSPICE using the CNTFET model of [3]. This HSPICE model of the CNTFET is described in more detail in [8,25]. The VTCs of the STI in Fig. 14 are shown in Fig. 15, which demonstrates that the proposed STI design provides a larger NM. That is a positive feature for low-power supply circuits. Furthermore, the proposed STI achieves a rail-to-rail output swing in contrast to the conventional STI design. In the HSPICE simulation, two STIs are cascaded as a ternary buffer. The average power consumption is the average power consumed by the two STIs, while the average delay is the average of the sum of four terms, i.e., the delay from 0 to 1, the delay from 1 to 2, the delay from 2 to 1, and the delay from 1 to 0. HSPICE simulation shows that the PDP of the proposed CNTFET-based STI is 6.08×10^{-17} J, and the PDP of the STI in [11] is 2.07×10^{-16} J. The proposed CNTFET-based STI achieves more than 300% performance improvement over [11] in terms of PDP.

Fig. 18. Schematic diagram of ternary decoder.

3.5 CNTFET based ternary gate design

As mentioned in the subsection 2.1, there are three inverters in the general ternary inverter system, which are NTI, STI, and PTI [19]. Figure 14 shows the proposed STI design. The NTI and PTI designs are shown in Fig. 16, where Fig. 16(a) shows the CNTFET-based NTI schematic diagram. The threshold voltage of T1 is 0.289 V, while the threshold voltage of T2 is -0.557 V. When the input voltage is below 0.3 V (i.e., logic 0), the output voltage is 0.9 V. As soon as the input voltage exceeds 0.3 V, T1 is ON and T2 is OFF, and the output voltage will be zero. For the CNTFET-based PTI shown in Fig. 16(b), the threshold voltage of T1 is 0.557 V and the threshold voltage of T2 is -0.289 V. Therefore, only when the input voltage is higher than 0.6 V, the output voltage is zero. The outputs of NTI and PTI correspond to y_0 and y_2 , as given previously in Eq. (2). Figure 17 shows the symbols of NTI, STI, and PTI.

The ternary gates presented in this section can be used for designing ternary arithmetic circuits such as ternary adders and multipliers. As required for these circuits, a new design of the ternary decoder is presented in Fig. 18. The ternary decoder is a one-input, three-output combinational circuit and generates unary functions for an input x . The response of the ternary decoder to the input x is given by

$$X_k = \begin{cases} 2, & \text{if } x = k \\ 0, & \text{if } x \neq k \end{cases} \quad (8)$$

where k can take logic values of 0, 1, or 2. The decoder consists of a PTI gate, two NTI gates, and a NOR gate, as shown in Fig. 18.

The logic expressions of the ternary NAND and NOR gates are given in Eqs. (3) and (4). The circuits and symbols for the two-input ternary NAND and ternary NOR are shown in Figs. 19(a) and (b), respectively. Each of these two gates consists of ten CNTFETs, with three different chiralities. They are essentially the same as their binary CMOS counterparts, except for the transistors of different threshold voltages. In these two gates, similar to the STI circuit of Fig. 14, the transistors with diameters of 1.487, 0.783, and 1.018 nm have threshold voltages of 0.289, 0.559, and 0.428 V, respectively, as established using Eq. (6). HSPICE simulation is confirmed the correctness of these designs with Tables 3 and 4.

One of the main advantages of ternary logic is that it reduces the number of required computation steps. Since each signal can have three distinct values, the number of digits required in a ternary family is $\log_3 2$ times less than required in binary logic. Therefore, if we consider an N -bit binary adder, then the corresponding ternary adder has $\lceil \log_3 2N \rceil$ digits, where $\lceil x \rceil$ represents the integer nearest to x and greater than x (i.e., the ceiling function).

A ternary half adder (HA) is then designed to verify the correctness of the proposed CNTFET-based design. The truth table of the ternary adder is given in Table 5 and the output equations for the HA can be derived from the Table 5 as

$$Sun = A_2 B_0 + A_1 B_1 + A_0 B_2 + 1 \bullet (A_1 B_0 + A_0 B_1 + A_2 B_2) \quad (9)$$

Fig. 19. Proposed carbon nanotube field-effect transistor-based NAND and NOR gates. (a) Schematic diagram of two-input NAND. (b) Schematic diagram of two-input NOR. (c) Symbols of NAND and NOR.

$$\text{Carry} = 1 \bullet (A_2 B_1 + A_2 B_2 + A_1 B_2) \quad (10)$$

where A_k and B_k denote the output of the inputs A and B from the decoder shown in Fig. 18.

The schematic diagram of the HA proposed in [26] is shown in Fig. 20. Two decoders generate the unary output signals for inputs A and B, while the logic gates compute the functions given by Eqs. (9) and (10). The so-called Tbuffer of Fig. 20 represents a level shifter and its logic function is given by

$$\text{Out} = \begin{cases} 1, & \text{if } in = 1, 2 \\ 0, & \text{if } in = 0 \end{cases} \quad (11)$$

where in is the input of the T gate and Out is the output of the T gate.

The transient response of the ternary HA design based on CNTFETs is shown in Fig. 20. Simulation results are consistent with the truth table given in Table 5.

Fig. 20. Transient response of the ternary half adder.

The ternary logic achieves significant savings in PDP compared with the ternary logic family with resistors proposed in [11]. By replacing ternary gates with binary gates in the internal logic, the proposed design also achieves power and delay savings due to the reduced number of transistors in the binary gates. Note that by replacing the external resistors with transistors, a significant saving in area is also achieved. Therefore, the proposed ternary design is a fast and low-power solution to digital computation compared with the existing conventional ternary logic families, as well as the binary implementation. The simulation results confirm that the ternary logic based haf adder's PDP is reduced by 90% compared with the existing logic families for arithmetic circuits [23], which implies that the ternary logic is a good solution to low power and high speed digital system design.

4. SRAM CELL DESIGN USING CNTFET

Design of fast and power efficient memory structures continues to be of the highest priority, and ballistic transport operation and low off current make the CNTFET a suitable device for high performance and increased integration density of SRAM design. Moreover, the MOSFET-like model of the CNTFET is likely to be scalable down to 10 nm channel length, thus providing a substantial performance and power improvement compared to the MOSFET model (with minimum channel length of 32 nm [3]). Therefore, a SRAM design implemented using CNTFETs requires a significantly smaller area than its CMOS counterpart. A resistive-load CNTFET-based SRAM cell has been proposed in [27]. However, large off-chip resistors (i.e. 100 MΩ) are needed in the configuration due to the current requirements of the CNTFETs. This resistive-load CNTFET-based SRAM cell design is modified with P-type transistors as active load to address this problem as proposed in this paper.

The use of transistors with multiple threshold voltages (i.e. a so-called multi-threshold design) is widely utilized in today's CMOS circuits to improve performance. The threshold voltage can be changed by applying different bias voltage to the bulk terminal of the CMOS transistors. The threshold voltage of CNTFET is determined by the CNT diameter as described in the previous Section. Therefore, CNTFETs with different threshold voltages can be accomplished by growing CNTs with different diameters (chiralities). In this paper, a CNTFET-based SRAM cell design

Fig. 22. Static noise margin of the static random access memory (SRAM) cell with (a) different PCNTFET chirality vectors; (b) different NCNTFET chirality vectors. CNTFET: carbon nanotube field-effect transistor.

For a CMOS SRAM cell with a transistor length of 32 nm and similar circuit performance to the CNTFET SRAM cell proposed in this section, the widths of MP5, MN3, and MN1 are found to be 80 nm, 160 nm, and 120 nm, respectively. Therefore, there are two 80/32 nm PMOS transistors, two 160/32 nm NMOS transistors and two 120/32 nm NMOS transistors in the CMOS SRAM cell. Compared to the CMOS at 32 nm feature size, the CNTFET-based SRAM cell has two 40/20 nm P-CNTFETs, two 80/20 nm N-CNTFETs, and two 60/20 nm N-CNTFETs. These transistors are used in the next section to establish the best operation under the optimized threshold voltages for the dual-diameter CNTFET-based SRAM cell.

4.2 Dual-chirality SRAM cell design

Since the threshold voltage of CNTFET can be controlled by adjusting tube's diameter, the design of CNTFET based circuits with different threshold voltages is possible because CNTs can be grown with different diameters [11,30,31]. In this paper, N-type and P-type CNTFETs use CNTs that have different chirality vectors for the best (optimized) performance. However, all N-type CNTFETs use CNTs with the same chirality vector and all P-type CNTFETs use the same chirality vector as well (the dual-

diameter arrangement is used for simplicity, although additional threshold voltages could also be utilized by using CNTs' different diameters in the transistors).

A new index is defined for the CNTFET-based SRAM design, and it is given by the triplet (np, nn, m) , where np and nn represent the first chirality vector " n " of the PCNTFETs and NCNTFETs, respectively, and m is the common second chirality vector " m " of the two CNTFETs [32,33]. For example, a SRAM cell with (16, 0) PCNTFETs and (19, 0) NCNTFETs is represented by the index triplet (16, 19, 0). The difference in chirality between N-type and P-type CNTFETs must also take into account the performance of the SRAM memory cell. As for CMOS SRAM, the threshold voltage of the pull-up P-type FETs (MP5 and MP6 shown in Fig. 21(b)) have a close relationship with the SNM of the SRAM cell (the SNM is defined as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit [34]). The SNM is commonly used as a metric for static stability of a SRAM cell [35].

To investigate the SNM of the proposed dual-diameter CNTFET SRAM, extensive simulations have been performed on CNTFET SRAM cells with index triplets of (10, 19, 0), (13, 19, 0), (16, 19, 0), (19, 19, 0), and (22, 19, 0) for the transistors. Figure 22 shows the simulation results of the read SNM of the SRAM cell at 0.9 V power supply and room temperature. For the 6T SRAM cell configuration in Fig. 21, the worst-case stability condition occurs when the cell is accessed for read operation, i.e. the read SNM is lower than the hold SNM. Simulation has shown that as the chirality vector of the PCNTFETs changes from (10, 0) to (22, 0), then the SNM of the CNTFET SRAM is increased. As shown in Fig. 22(a), the read SNM of the CNTFET SRAM is larger than for the CMOS SRAM at 32 nm feature size. Simulation has also been performed by changing the chirality vector of the N-type CNTFETs in the range from (10, 0) to (22, 0). As shown in Fig. 22(b), the values of the read SNM of the CNTFET SRAM change little as the chirality vectors of the N-type CNTFETs change. Therefore, for best stability, the chirality vector of the PCNTFETs must be adjusted.

The stability of the SRAM cell can be increased by decreasing the absolute value of the threshold voltage of the pull-up transistor and controlling its chirality vector. However, there is a conflicting constraint between performance and stability. At a better ability to hold data, it is also harder to write new data into the SRAM cell, i.e. it takes more time to write new data. To find the optimum chirality for both PCNTFETs and NCNTFETs, both the SNM and the write time must be considered. Table 5 shows the SNM and the write time of the CNTFET SRAM cell with different threshold voltages of the PCNTFET at 0.9 V power supply and room temperature. Both the SNM and the write time increase with decrease of the absolute value of the threshold voltage of the pull-up transistor. For a highly stable and low delay design, a high SNM and a fast write time are desired. Therefore, the SNM is divided by the write time to find the best threshold voltage of the PCNTFET for both high SNM and fast write time. As shown in Table 5, when the threshold voltage of the PCNTFET is 0.343 V for a (16, 19, 0) SRAM cell, the ratio between the SNM and the write time is the highest among those CNTFET SRAM cells listed in Table 5. Therefore, the (16, 19, 0) SRAM cell is selected for best overall performance. It is also shown in Table 5 that the ratio between the SNM and the write time for the CNTFET SRAM cell is significantly higher than for the CMOS SRAM cell, i.e. high stability is attained at a low write time.

4.3 Metrics for memory cell

A novel is required to comprehensively assess the performance as a function of delay, stability with respect to noise, and power

Table 5. SNM and write time of the SRAM cells at 0.9 V power supply and room temperature.

SNM (mV)	Vth of N-type FET (mV)	Vth of P-type FET (mV)	SNM (mV)	Write time (ps)	SNM/write time (mV/ps)
(10, 19, 0) CNTFET SRAM cell	289	-550	125	20.51	6.09
(13, 19, 0) CNTFET SRAM cell	289	-422	175	23.45	7.46
(16, 19, 0) CNTFET SRAM cell	289	-343	206.3	24.97	8.26
(19, 19, 0) CNTFET SRAM cell	289	-289	244	29.70	8.21
(22, 19, 0) CNTFET SRAM cell	289	-250	262.5	32.25	8.13
32 nm CMOS SRAM cell	180	-180	81.3	24.64	3.29

SNM: static noise margin, SRAM: static random access memory, CNTFET: carbon nanotube field-effect transistor.

Table 6. SPR of SRAM cells at 0.9 V power supply and room temperature.

SRAM cell	SNM (mV)	SINM (uA)	Write power (uW)	Write delay (ps)	SPR (1/s)
CMOS SRAM cell	117.6	34.33	29.56	24.64	4.142e+9
CNTFET SRAM cell	206.3	31.53	16.47	24.97	1.582e+10

SNM: static noise margin, SRAM: static random access memory, SPR: static power noise margin to power delay product ratio, CNTFET: carbon nanotube field-effect transistor.

Fig. 23. Write time distribution of complementary metaloxide semiconductor (CMOS) and carbon nanotube field-effect transistor (CNTFET) static random access memory (SRAM) cells.

dissipation within a comprehensive metric. HSPICE simulations are performed using the Stanford CNTFET model [3] and the Berkeley Predictive 32 nm CMOS model [29] to compare the CNTFET and CMOS 6T SRAM cells. It has been shown in [35] that both the SNM and the static current noise margin (SINM) must be used to address the static stability of a SRAM cell. Therefore, SNM and SINM are multiplied together to yield a comprehensive figure of merit as the static power noise margin (SPNM). The PDP is an important and often used to measure and compare the circuits. It has been shown in articles [8,25] that the CNTFET has very high on/off current ratio compared with its CMOS counterpart. Therefore, the standby power of the CNTFET SRAM is significantly lower than for the CMOS SRAM. However, it is also important to address write power dissipation as the power dissipated by a memory cell during the write operation is higher than the power dissipated during the read operation due to the full swing charge and discharge on the bitlines during the write operation. Therefore, the PDP of the SRAM cell proposed in this paper is the product of the write power and the write delay.

The new comprehensive performance metric proposed in [36]

Fig. 24. Standby power dissipation distribution of complementary metaloxide semiconductor (CMOS) and carbon nanotube field-effect transistor (CNTFET) static random access memory (SRAM) cells.

includes delay, stability, and power. It is given by dividing the SPNM by the PDP and this is referred to as the SPNM to PDP ratio (SPR). The SPR (in units of 1/secs) can be expressed as $SPR = (SNM \times SINM) / (write\ power \times write\ delay)$ and provides a metric for high stability, low delay and low power in the operation of a memory cell. SPR is also versatile as it can be used to assess performance under different operational conditions, such as standby and write. Table 6 shows the SNM, SINM, write power, and write delay of the CMOS SRAM cell and the CNTFET SRAM cell at 0.9 V power supply and room temperature. As shown in Table 6, the CNTFET SRAM cell is designed to have the same write delay as the CMOS SRAM cell. The decrease of the write delay implies that it is easier to write data into a SRAM cell, thus making stability degrade. Also, the improvement in delay performance usually requires a larger transistor size, thus increasing power consumption. Therefore, to comprehensively assess performance as a function of delay and stability with respect to noise and power dissipation, a new metric must be used. The metric SPR provides such a metric for a SRAM cell in terms of delay, stability, and power. Table 6 confirms that the SPR of the CNTFET 6T SRAM cell is four times higher than its CMOS counterpart, hence attaining low power, high stability, and low delay within the comprehensive metric provided by the SPR under write conditions.

4.4 Impact of variations

Systematic and random variations in process, PVT are posing a major challenge to nanoscale CMOS integrated circuits. Systematic variations in PVT are shared among all devices and have become a significant concern to the parametric yield in terms of energy and delay.

In CMOS process, random process variations often cause geo-

metric variations in the gate (length, width, and thickness) as well as gate oxide thickness. In short channel devices, a variation in channel length also induces change in threshold voltage due to the drain-induced barrier lowering (DIBL) [37]. These variations still exist even in CNTFET. However, due to the cylindrical geometry, a variation in the gate oxide thickness that strongly affects the drive current and capacitance of CMOS transistors has a negligible impact on the CNTFET's operation. The gate width in CNTFET is not the effective channel width of the transistor. This only depends on the CNT diameter and the number of tubes under the gate and does not affect the drive current. As in [38] only the CNT diameter has the strongest impact on the CNTFET performance while other process variations have only a small impact. Monte Carlo simulation by HSPICE has been performed to investigate the impact of the random variations on the delay and power of the CNTFET and CMOS SRAM cells at 0.9 V power supply and room temperature. Figure 23 shows the distribution of the write time of the CNTFET and CMOS 6T SRAM cells under geometric parameters with random changes. All simulation results are normalized to the SRAM's write time under no process variation. Figure 23 shows that the write time of the proposed dual-diameter CNTFET 6T SRAM cell has much better tolerance to process variations compared to its CMOS counterpart. Figure 24 shows the distribution of the standby power consumption of the CNTFET and CMOS 6T SRAM cells. Likewise the previous cases, all simulated results are normalized to the SRAM cell standby power consumption under no process variation. Due to the significantly low standby power consumption and fewer parameters causing changes in power consumption, the CNTFET SRAM cell shows a significantly better tolerance to process variations.

5. CONCLUSIONS

As dimensional scaling of CMOS transistors is reaching their fundamental physical limits, various researches have been actively carried out to find an alternative way to continue to follow Moore's law. Among these efforts, CNTFETs turned out to be the most promising candidate. To test the feasibility of the CNTFET technology, a different type of logic circuits including combinational and memory elements have been investigated. To maximize the benefits of the CNTFET technology, ternary logic circuits have been reviewed with test cases. In more detail, the CNTFET based combinational logic gates have been compared with the counter part of CMOS bulk CMOS technology in terms of power and delay and ternary logic gates performance have been assessed and compared with CMOS binary logic circuits. Since the memory component of the modern VLSI systems becomes more important, SRAM cell has been designed using CNTFET and its performance has been assessed in terms of write/read time, SNM. A new comprehensive metric for SRAM cells denoted as SPR was used in this paper; SPR is a composite and versatile performance measure in terms of stability, power, and delay.

In all of the attempts from combinational logic gate and ternary logic gate to SRAM memory cell, CNTFET based digital circuits show a significant improvements compared to the design of nanoscale CMOS counterparts in terms of power consumption and area. The proposed dual-diameter CNTFET SRAM cell has a better SPR under write operation than its CMOS counterpart cell. Moreover, simulation has shown that the proposed dual-diameter CNTFET based SRAM design has significant lower sensitivity to process, voltage, and temperature variations.

Based on the review and observation of the CNTFET based digital logic circuits, it is fair to say that CNTFET based integrat-

ed circuits design is a viable solution to replace the conventional bulk CMOS technology and it turns out to be an effective choice of future technology if manufacturability issues such as controllability of metallic/semiconducting property and metallic contacts are taken care of.

REFERENCES

- [1] R. C. Baumann, IEEE Trans Dev Mat Rel **1**, 17 (2001) [http://dx.doi.org/10.1109/7298.946456].
- [2] M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar, and K. Bernstein, IEEE International Electron Devices Meeting (Washington, DC 2005 Dec. 5) p. 9. [http://dx.doi.org/10.1109/IEDM.2005.1609253].
- [3] Stanford University Nanoelectronics Group. *Stanford University CNTFET Model*. Retrieved from http://nano.stanford.edu/model.php?id=23.
- [4] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, IEEE Trans Electron Devices **50**, 1853 (2003) [http://dx.doi.org/10.1109/ted.2003.815366].
- [5] A. Akturk, G. Pennington, N. Goldsman, and A. Wicken-den, IEEE Trans Nanotechnol **6**, 469 (2007) [http://dx.doi.org/10.1109/tnano.2007.896968].
- [6] H. Hashempour and F. Lombardi, IEEE Des Test Comput **25**, 178 (2008) [http://dx.doi.org/10.1109/mdt.2008.34].
- [7] Y. M. Lin, J. Appenzeller, J. Knoch, and P. Avouris, IEEE Trans Nanotechnol **4**, 481 (2005) [http://dx.doi.org/10.1109/tnano.2005.851427].
- [8] J. Deng and H. S. P. Wong, IEEE Trans Electron Devices **54**, 3195 (2007) [http://dx.doi.org/10.1109/ted.2007.909043].
- [9] J. Guo, A. Javey, H. Dai, S. Datta, and M. Lundstrom, eprint arXiv:cond-mat/0309039 (2003).
- [10] K. K. Kim and Y. B. Kim, IEEE Trans Very Large Scale Integr (VLSI) Syst **17**, 517 (2009) [http://dx.doi.org/10.1109/TVLSI.2008.2007958].
- [11] A. Raychowdhury and K. Roy, IEEE Trans Nanotechnol **4**, 168 (2005) [http://dx.doi.org/10.1109/tnano.2004.842068].
- [12] S. Lin, Y. B. Kim, and F. Lombardi, Proceedings of the 52nd IEEE International Midwest Symposium on Circuits and Systems (Cancun, Mexico 2009 Aug. 2-5) p. 435. [http://dx.doi.org/10.1109/MWSCAS.2009.5236063].
- [13] T. P. Haraszti, *CMOS Memory Circuits* (Kluwer Academic Publishers, Boston, 2000).
- [14] F. Ricci, L. T. Clark, T. Beatty, W. Yu, A. Bashmakov, S. Demmons, E. Fox, J. Miller, M. Biyani, and J. Haigh, Symposium on VLSI Circuits (Kyoto, Japan 2005 Jun. 16-18) p. 12. [http://dx.doi.org/10.1109/VLSIC.2005.1469322].
- [15] A. P. Chandrakasan, W. J. Bowhill, and E. Fox, *Design of High-Performance Microprocessor Circuits* (IEEE Press, New York, 2001) p. 290-296.
- [16] K. K. Kim and Y. B. Kim, IEEE International Symposium on Circuits and Systems (New Orleans, LA 2007 May 27-30) p. 1161. [http://dx.doi.org/10.1109/ISCAS.2007.378256].
- [17] M. Mukaidono, IEEE Trans Comput **C-35**, 179 (1986) [http://dx.doi.org/10.1109/TC.1986.1676738].
- [18] T. Araki, H. Tatsumi, M. Mukaidono, and F. Yamamoto, Proceedings of the 28th International Symposium on Multiple-Valued Logic (Fukuoka, Japan 1998 May 27-29) p. 289. [http://dx.doi.org/10.1109/ISMVL.1998.679472].
- [19] P. C. Balla and A. Antoniou, IEEE J Solid-State Circuits **SC-19**, 739 (1984) [http://dx.doi.org/10.1109/JSSC.1984.1052216].
- [20] A. Heung and H. T. Mouftah, IEEE J Solid-State Circuits **SC-20**, 609 (1984) [http://dx.doi.org/10.1109/JSSC.1985.1052354].
- [21] D. A. Rich, IEEE Trans Comput **C-35**, 99 (1986) [http://dx.doi.org/10.1109/TC.1986.1676727].

- [22] Y. Yasuda, Y. Tokuda, S. Zaima, K. Pak, T. Nakamura, and A. Yoshida, *IEEE J Solid-State Circuits* **SC-21**, 162 (1986) [<http://dx.doi.org/10.1109/JSSC.1986.1052493>].
- [23] S. Lin, Y. B. Kim, and F. Lombardi, *IEEE Trans Nanotechnol* **10**, 217 (2011) [<http://dx.doi.org/10.1109/TNANO.2009.2036845>].
- [24] J. Appenzeller, *Proc IEEE* **96**, 201 (2008) [<http://dx.doi.org/10.1109/jproc.2007.911051>].
- [25] J. Deng and H. S. P. Wong, *IEEE Trans Electron Devices* **54**, 3186 (2007) [<http://dx.doi.org/10.1109/ted.2007.909030>].
- [26] A. P. Dhande and V. T. Ingole, *Proceedings of the 3rd International Conference: Sciences of Electronic, Technologies of Information and Telecommunications* (Tunisia 2005 Mar. 17-21).
- [27] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, *Science* **294**, 1317 (2001) [<http://dx.doi.org/10.1126/science.1065824>].
- [28] S. Lin, Y. B. Kim, F. Lombardi, and Y. J. Lee, *Proceedings of the International SoC Design Conference* (Busan, Korea 2008 Nov. 24-25) p. 1168. [<http://dx.doi.org/10.1109/SOCD.2008.4815599>].
- [29] Nanoscale Integration and Modeling (NIMO) Group (Nov. 15, 2008). *Berkeley Predictive Technology Model*. Retrieved from <http://ptm.asu.edu/>.
- [30] Y. Li, W. Kim, Y. Zhang, M. Rolandi, D. Wang, and H. Dai, *J. Phys. Chem. B* **105**, 11424 (2001) [<http://dx.doi.org/10.1021/jp012085b>].
- [31] Y. Ohno, S. Kishimoto, T. Mizutani, T. Okazaki, and H. Shinohara, *Appl. Phys. Lett.* **84**, 1368 (2004) [<http://dx.doi.org/10.1063/1.1650554>].
- [32] C. Geunho, F. Lombardi, and K. Yong-Bin, *Proceedings of the IEEE 25th International Symposium on Defect and Fault Tolerance in VLSI Systems* (Kyoto, Japan 2010 Oct. 6-8) p. 289. [<http://dx.doi.org/10.1109/DFT.2010.42>].
- [33] G. Cho, Y. B. Kim, and F. Lombardi, *IEEE Trans Dev Mat Rel* **11**, 263 (2011) [<http://dx.doi.org/10.1109/tdmr.2011.2123896>].
- [34] E. Seevinck, F. J. List, and J. Lohstroh, *IEEE J Solid-State Circuits* **SC-22**, 748 (1987) [<http://dx.doi.org/10.1109/JSSC.1987.1052809>].
- [35] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, *IEEE J Solid-State Circuits* **41**, 2577 (2006) [<http://dx.doi.org/10.1109/jssc.2006.883344>].
- [36] S. Lin, Y. B. Kim, and F. Lombardi, *IEEE Trans Nanotechnol* **9**, 30 (2010) [<http://dx.doi.org/10.1109/tnano.2009.2025128>].
- [37] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, *Proc IEEE* **91**, 305 (2003) [<http://dx.doi.org/10.1109/jproc.2002.808156>].
- [38] B. C. Paul, S. Fujita, M. Okajima, T. H. Lee, H. S. P. Wong, and Y. Nishi, *IEEE Trans Electron Devices* **54**, 2369 (2007) [<http://dx.doi.org/10.1109/ted.2007.901882>].