The Short Channel Effect Immunity of Silicon Nanowire SONOS Flash Memory Using TCAD Simulation

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Received January 22, 2013; Revised March 15, 2013; Accepted March 21, 2013

Silicon nanowire (SiNW) silicon-oxide-nitride-oxide-silicon (SONOS) flash memory devices were fabricated and their electrical characteristics were analyzed. Compared to planar SONOS devices, these SiNW SONOS devices have good program/erase (P/E) characteristics and a large threshold voltage (V_T) shift of 2.5 V in 1ms using a gate pulse of +14 V. The devices also show excellent immunity to short channel effects (SCEs) due to enhanced gate controllability, which becomes more apparent as the nanowire width decreases. This is attributed to the fully depleted mode operation as the nanowire becomes narrower. 3D TCAD simulations of both devices show that the electric field of the junction area is significantly reduced in the SiNW structure.

Keywords: SiNW, SONOS flash memory, DIBL, TCAD simulation

1. INTRODUCTION

The scaling of conventional planar flash memory is expected to end beyond the sub-20 nm technology node due to concerns about lithography, the coupling ratio, and the crosstalk interface. Future memory requires faster program/erase speed, longer data retention, and higher storage capacity, at a lower cost. SONOS flash memory devices have been considered the most promising candidate for implementing low-voltage and high-density non-volatile semiconductor memory [1]. However, short channel effects (SCEs) become apparent as the memory cell is scaled down. To solve the SCE problem, various 3D structures for SONOS devices have been reported [2,3]. In particular, nanowire transistors have generated much recent research interest [4-7] because of their potential to replace conventional planar structures in scaling CMOS devices to gate length of 10 nm or less. With the impending tunneling limit of gate oxides at a thickness of 1 nm or slightly less, it is difficult to scale bulk MOSFETs to gate lengths

of less than 20 nm with acceptable SCEs [8]. Nanowire transistors, which are basically gate-all-around devices, offer superior electrostatic control of the channel to suppress SCEs. This paper reports the fabrication of SiNW and planar SONOS flash memories, and analysis of the electrical characteristics. To uncover the reason for good SCE immunity in SiNW SONOS devices, both devices were examined with 3D TCAD simulations.

2. EXPERIMENTS

A schematic of the SiNW gate-all-around (GAA) SONOS flash memory device and its process flow are shown in Fig. 1. A p-type (100) bulk wafer was used as the starting material. One distinctive feature in forming SiNW from bulk Si is the one-step etching route to pattern the SiNW and to isolate the adjacent FETs. A photolithography process using 0.18 μm technology was employed to define the SiNW. To achieve a minimum feature size for the SiNW, photoresist ashing, in part by oxygen plasma, was performed as described in another study [9]. Afterwards, the 180-nm line width was reduced to 30 nm. In the one-step etching route, in-situ generated CF_4 -based polymer begins to passivate the exposed Si surface during reactive ion etching (RIE) through the Bosch process [10].

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Fig. 1. Schematic of SiNW SONOS flash memory.

Fig. 2. (a) Tilted SEM image showing the suspended SiNW after the Bosch process and (b) cross-sectional TEM image of the SiNW inside the poly-Si gate.

In this process, isotropic etching is used exclusively to completely separate the SiNW from the bulk substrate. Therefore, enhanced reproducibility can be expected. Afterward, sacrificial oxidation was employed to alleviate etching damage. Next, ONO layers were deposited with thickness of 4/8/12 nm using silicon nitride (Si_3N_4) as the trapping layer. Additionally, an n+ in-situ doped poly-silicon layer was deposited to surround the SiNWs to fabricate the gate electrode. To pattern the gate, photoresist ashing was also used, and a gate length of 25 nm was ultimately achieved. 2-nm-thick oxide spacers were then formed for the subsequent formation of the source and drain (S/D). After patterning the gate, the S/D was doped with arsenic, and the dopants were activated using rapid thermal annealing (RTA) at 1,000 °C for 3 sec. Finally, forming gas annealing was applied. Fig. 2 shows a cross-sectional transmission electron microscopy (TEM) image of the 25-nm gate length (L_G). The L_G of the fabricated device ranged from 25 to 125 nm. The major electrical characteristics of the devices were measured using a semiconductor parameter analyzer (HP4156C). The structure of the SONOS device was recreated by Synopsys TCAD tools with a structure device editor (SDE) and Sentaurus device, which is an

Fig. 3. The measurement results of program and erase characteristics of the fabricated SiNW SONOS flash memory. The gate length is 25 nm and the NW width is 20 nm.

Fig. 4. Experimental results of V_G - I_D characteristic of planar and SiNW SONOS flash memory devices.

advanced multidimensional simulator capable of simulating the electrical, thermal, and optical characteristics of silicon-based and compound semiconductor devices.

3. RESULTS AND DISCUSSION

Figure 3 shows the measured program/erase characteristics of the fabricated SiNW SONOS flash memory ($L_G = 25$ nm and NW width = 20 nm). A Fowler-Nordheim tunneling mechanism was employed to measure how the memory of the cell performed by grounding the source and drain and stressing the gate. Based on the programming characteristics, the SiNW devices exhibit a large threshold voltage (V_T) shift of 2.5 V within 1 ms using a pulse of +14 V on the gate. However, the SiNW device requires more time to erase what is written in programming. This erase process is known to be slow due to the lower tunneling probability of holes than that of the electrons used in programming.

Figure 4 shows the experimental results of the gate voltage-drain current (V_G - I_D) measurements in the fabricated SiNW and planar SONOS devices with a 25 nm L_G . The SiNW device shows superior short-channel immunity with a drain-induced barrier leakage (DIBL) of 200 mV/V and subthreshold slope (SS) of 102 mV/dec. DIBL is defined as $(V_{T,lin} - V_{T,sat})/0.95$ V, where $V_{T,lin}$ and $V_{T,sat}$ are the threshold voltage (V_T) at drain biases (V_D) of 0.05 and 1 V, respectively. SS was extracted at $V_D = 0.05$ V. The ON-state current (I_{on}) is 7 μ A at $V_G - V_{T,sat} = 1$ V and $V_D = 1$ V. This can be enhanced by reducing the gate oxide thickness further and optimizing S/D.

Fig. 5. TCAD-simulated structure of (a) SiNW and (b) planar SONOS flash memory devices.

To understand the origins of the excellent performance of SiNW SONOS devices, simulations were performed using a commercial 3D TCAD tool. Figure 5 shows the overall structure of the SiNW and planar SONOS devices. The simulation results are similar to the experimental data, as shown in Fig. 6. Compared with planar SONOS devices, SiNW SONOS devices show excellent SCE immunity, with good DIBL and SS performance.

The simulated L_G dependencies of the DIBL and SS of the SiNW and planar devices of various widths are presented in Fig. 7. The SCEs in the GAA FETs are effectively suppressed upon reducing the SiNW dimensions. Compared with a similar study based on a silicon-on-insulator (SOI) substrate [11], these results show that reasonable device characteristics and SCEs can be attained from the SiNW devices even when implemented on bulk Si due to the superior electrostatic nature of the GAA. The proposed process based on the bulk Si can be considered a promising method for creating highly scaled SiNW devices using a cost-effective process.

Figure 8 shows the results of the TCAD simulation of the electric field distribution of planar and SiNW SONOS flash memory devices. The electric field of the junction area is significantly reduced in the SiNW structure, as indicated with red circles.

4. CONCLUSIONS

The fabrication of silicon nanowire (SiNW) silicon-oxide-nitride-oxide-silicon (SONOS) flash memory devices and the analysis of their electrical characteristics have been described. Compared with planar SONOS devices, SiNW SONOS devices have good P/E characteristics and show excellent SCE immunity due to enhanced gate controllability. In addition, the SiNW SONOS devices exhibit improved SCE immunity in accordance with the decrease in nanowire width. This is known to be due to the fully depleted mode operation as the nanowire becomes narrower. To uncover the reason for good SCE immunity in SiNW SONOS devices, both devices examined with TCAD simulations. The results show that the electric field of the junction area is significantly reduced in the SiNW structure.

Fig. 6. Simulation results for the V_G - I_D characteristics of planar and SiNW SONOS flash memory devices.

Fig. 7. Simulation results of (a) DIBL and (b) SS versus L_G of SiNW and planar devices of various widths.

Fig. 8. The electric field distribution of (a) planar and (b) SiNW SONOS flash memory devices.

ACKNOWLEDGMENTS

This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2012R1A1A3018050) and by the Ministry of Knowledge Economy (MKE) and the Korea Institute for Advancement of Technology (KIAT) through the Workforce Development Program in Strategic Technology.

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