OPAMP Design Using Optimized Self-Cascode Structures

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A new CMOS analog design methodology using an independently optimized self-cascode (SC) is proposed. This idea is based on the concept of the dual-workfunction-gate MOSFETs, which are equivalent to SC structures. The channel length of the source-side MOSFET is optimized, to give higher transconductance (g_m) and output resistance (r_{out}). The highest g_m and r_{out} of the SC structures are obtained by independently optimizing the channel length ratio of the SC MOSFETs, which is a critical design parameter. An operational amplifier (OPAMP) with the proposed design methodology using a standard digital 0.18- μm CMOS technology was designed and fabricated, to provide better performance. Independently g_m and r_{out} optimized SC MOSFETs were used in the differential input and output stages, respectively. The measured DC gain of the fabricated OPAMP with the proposed design methodology was approximately 18 dB higher, than that of the conventional OPAMP.

Keywords: Operational amplifier, Self-cascode, Analog design methodology, Circuit optimization

1. INTRODUCTION

Modern CMOS technologies continue to scale down to the nanometer regime, and the power supply has also reduced to an ultra-low voltage of 0.5 V. Although this evolution in CMOS technology is suitable for digital circuitry, this is not so beneficial for analog circuits [1-4]. Excessively-scaled device dimensions show reduced output resistance, due to channel length modulation (CLM). Moreover, enhancing the analog circuit performance using the general analog circuit design methodology, such as the use of long channel devices and conventional cascode configurations, is difficult, due to threshold voltages (V_{TH}) and output swing limitations.

The self-cascode (SC) structure is widely used to reduce the CLM effect, and is utilized in the design of a low-voltage operational transconductance amplifier (OTA), which shows high

DC gain and output voltage swing [4-6]. On the other hand, the large channel width and length (W/L) ratio of two MOSFETs with a SC structure is one of its disadvantages. Asymmetric- V_{TH} SC structures using low- V_{TH} MOSFET have been proposed [7]. This approach requires a lower W/L ratio, but additional fabrication processing steps are unavoidable. Currently, an asymmetric- V_{TH} SC structure can be easily implemented, using forward body-biasing techniques in a triple-well technology, or silicon-on-insulator (SOI) technology [8,9]. The SC structure can also be used for an indirect compensation technique, for high speed operational amplifier (OPAMP) [8,10]. The dual-workfunction-gate (DWFG) MOSFET is a newly introduced transistor with an asymmetrically-doped poly-silicon gate, to increase the output resistance (r_{out}) and transconductance (g_m) [11]. The length of the source-side gate with a higher workfunction is an important variable for optimizing r_{out} and g_m . Surprisingly, the DWFG MOSFET is a similar concept to the SC structure, and can be applied to analog circuit design, but this technique requires complicated processing steps.

This paper proposes a new CMOS analog circuit design methodology, using SC structures and the DWFG concept. In the proposed method, the channel length of the SC structure in a

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standard digital CMOS technology is separately optimized for a higher g_m and r_{out} . Using this optimizing method, a two-stage OPAMP with higher gain was fabricated, and measured to verify the proposed idea. A 0.18- μm standard triple-well CMOS technology was used to both simulate, and fabricate the OPAMP, using the proposed design method.

This paper is organized as follows. Section 2 introduces the proposed analog design methodology, and its application to the design of a two-stage OPAMP. Section 3 presents the experimental results of a comparative study of the SC and equivalent single MOSFET. The measured performances of the fabricated two-stage OPAMP using the proposed design methodology are also summarized. Finally, the conclusions are reported in section 4.

2. EXPERIMENTS

This section describes the channel length optimization of the SC structures with respect to g_m and r_{out} , as well as the application of the proposed design methodology to the design of a two-stage OPAMP.

2.1 Analog design methodology using optimized self-cascode

Figure 1 shows the simulated g_m and r_{out} characteristics of the n-channel SC structure (nSC). The n-channel MOSFETs (nMOSFETs) of MNd and MNs are connected in series, and a forward body-bias for MNd, which is insufficient to turn on the parasitic body-source diode, is applied to reduce V_{TH} , without using a low- V_{TH} MOSFET. A forward body-bias is not possible for the conventional body grounded nMOSFET. Therefore, triple-well or SOI CMOS technology is required. A deep n-well was used to allow the body of the nMOSFET MNd to be slightly forward-biased. With $V_{CMN} = 0.6\text{ V}$, the V_{TH} of MNd is reduced by approximately 0.1 V. The total channel length ($L = L_s + L_d$) is 1.0 μm , and a channel width of 5.0 μm is used for both MNd and MNs. The SC structure is a well-known circuit configuration for low-voltage analog circuit design [4-7]. The nMOSFET MNs normally operates in the triode regime, and MNd operates in the saturation regime. The effective r_{out} of the nSC is approximately the triode resistance of MNs multiplied by the intrinsic gain of MNd ($r_{out,eff} \approx g_{m,MNd} \cdot r_{out,MNd} \cdot r_{out,MNs}$). Therefore, if the triode resistance of MNs increases, the effective r_{out} of nSC can be enhanced. If the V_{TH} of MNd is reduced, the drain-source voltage V_{DS} of MNs increases, and the operation of MNs moves from the triode to the saturation regime. Consequently, the effective r_{out} of nSC can be maximized, when V_{DS} of MNs approaches the overdrive voltage ($V_{OV} = V_{GS} - V_{TH}$) of MNs. The condition of Eq. (1) should be satisfied by forward-biasing the body of MNd to give the highest r_{out} and output voltage swing [7].

$$|V_{TH \cdot MNs}| - |V_{TH \cdot MNd}| \geq |V_{OV \cdot MNd}| \quad (1)$$

Figure 1 shows that both g_m and r_{out} are strong functions of the channel length of the source-side MOSFET MNs (L_s). The nSC with $L_s = 0.5\text{ }\mu\text{m}$ shows the highest r_{out} characteristics, compared to the equivalent single nMOSFET with $L = 1.0\text{ }\mu\text{m}$. The characteristics of g_m are different from those of r_{out} . The g_m of the nSC with $L_s = 0.5\text{ }\mu\text{m}$ is similar to that of the single nMOSFET with $L = 1.0\text{ }\mu\text{m}$, but when L_s is reduced below 0.5 μm , then g_m of the nSC begins to improve. The reason is as follows: the effective g_m of the nSC is dominated by the g_m of the source-side transistor MNs. Hence, a more enhanced g_m of the nSC with shorter L_s is

Fig. 1. Simulated g_m and r_{out} of nSC as a function of the channel length of the source-side MOSFET (L_s). The design parameters and bias conditions for simulation are annotated in the figure. The equivalent single nMOSFET has an identical channel width and length ($W/L = 5.0\text{ }\mu\text{m}/1.0\text{ }\mu\text{m}$).

observed. From Fig. 1, the nSC with $L_s = 0.2\text{ }\mu\text{m}$ shows the highest g_m .

Figure 2 shows the simulated g_m and r_{out} characteristics of the p-channel SC structure (pSC), as a function of L_s . A forward body-bias for p-channel MOSFET (pMOSFET) MPd is also applied to reduce $|V_{TH}|$. Therefore, pMOSFET with a separated n-well was used for MPd. With $V_{CMP} = 1.4\text{ V}$, $|V_{TH}|$ of MPd is reduced by approximately 0.1 V. The total channel length ($L = L_s + L_d$) is 1.0 μm , and a channel width of 20.0 μm is used for both MPd and MPs. The pSC with $L_s = 0.6\text{ }\mu\text{m}$ shows the highest r_{out} characteristics, compared to the equivalent single pMOSFET ($L = 1.0\text{ }\mu\text{m}$). On the other hand, the pSC with $L_s = 0.2\text{ }\mu\text{m}$ shows the highest g_m .

From Figs. 1 and 2, the shorter L_s of the nSC and pSC shows more enhanced g_m characteristics than the single n and pMOSFETs, because the source-side MOSFETs MNs and MPs determine the effective g_m of the SC structures. On the other hand, the largest r_{out} characteristics of the nSC are observed when the source and drain-side MOSFETs of the nSC have identical length ($L_s = L_d$). If the channel length of the source-side MOSFET L_s is less than 0.5 μm , $r_{out,MNs}$ decreases. Therefore, the effective r_{out} of nSC is reduced. If $L_s > 0.5\text{ }\mu\text{m}$, the V_{TH} reduction is no longer possible, due to the reverse short channel effect (RSCE) of the nMOSFET, as shown in Fig. 3 (a). In other words, nSC cannot satisfy the previously mentioned condition Eq. (1) to achieve a higher effective r_{out} . Another factor is that $r_{out,MNd}$ decreases, due to the short channel length. Therefore, $L_s = L_d$ shows the largest r_{out} of nSC. Fig. 3 (b) shows the V_{TH} difference between the source and drain-side MOSFETs (ΔV_{TH}) of the nSC and pSC structures. The pMOSFET also has RSCE, but it is less severe than that of nMOSFET, i.e. the ΔV_{TH} of the pSC is less sensitive than that of the nSC. The effective r_{out} tendency of the SC structure is dependent on the device characteristics in the adopted CMOS technologies. Figures. 1 and 2 show that the

Fig. 2. Simulated g_m and r_{out} of pSC as a function of the channel length of the source-side MOSFET (L_s). The design parameters and bias conditions for simulation are annotated in the figure. The equivalent single pMOSFET has an identical channel width and length ($W/L = 20.0 \mu\text{m}/1.0 \mu\text{m}$).

channel length of the source-side MOSFET (L_s) is a critical parameter for the g_m and r_{out} optimization of SC structures. Figs. 1 and 2 also show that the SC structures have different optimized L_s values for g_m and r_{out} , i.e., they should be independently optimized.

2.2 Application to the design of a two-stage OPAMPs

The OPAMP is a fundamental building block of many analog and mixed-signal systems. The design of the OPAMPs continues to pose a challenge, as the supply voltage and device channel length scale down with each generation of CMOS technology. The g_m or r_{out} optimized SC structures described in the previous subsection are applied to the two-stage OPAMP, as shown in Fig. 4. To enhance the performance of OPAMP, the g_m optimized SC MOSFETs ($L_s = 0.2 \mu\text{m}$) are used for the differential input pairs of the pSC MP1-MP2, and the r_{out} optimized pSC MOSFETs ($L_s = 0.6 \mu\text{m}$) are used in the current mirror MP3-MP5. In addition, the r_{out} optimized nSC MOSFETs ($L_s = 0.5 \mu\text{m}$) are used in the active load MN1-MN2 and 2nd stage common-source amplifier MN3. The tail current of the differential input stage is $20 \mu\text{A}$.

Figure 5 shows the simulated frequency response of both the conventional OPAMP with the equivalent single MOSFETs, and the OPAMP with the independently optimized SC MOSFETs. The DC gain of OPAMP with the optimized SC structures is 99 dB, which is 14 dB higher than that of the conventional OPAMP. The use of the g_m optimized pSC in the differential input stage helps achieve a higher unity-gain frequency f_t . The unity-gain frequency of OPAMP with the optimized SC is 9.85 MHz, which is 2 MHz higher than the 7.82 MHz of the conventional OPAMP.

The input-referred noise of the OPAMP can be reduced, by

Fig. 3. (a) V_{TH} roll-off curve of single nMOSFET against the channel length (L), (b) V_{TH} difference of the source and drain-side SC MOSFETs as a function of L_s , while maintaining the total channel length at $1.0 \mu\text{m}$.

Fig. 4. Circuit diagram of the two-stage OPAMPs using the optimized SC structures.

maximizing the transconductance of the differential input pairs for a given bias current [10]. The input-referred thermal noise voltage level of the proposed OPAMP is $18.9 \text{ nV}/(\text{Hz})^{1/2}$, which is 26% lower than that of the conventional OPAMP with the single MOSFETs.

The common-mode rejection ratio (CMRR), and the power-supply rejection ratio (PSRR) of the differential pairs, are proportional to the output resistance of the tail current source. Therefore, the r_{out} optimized pSC MP4 in Fig. 4 helps enhance the CMRR and PSRR of the OPAMP. The PSRR of OPAMP with the optimized SC is largely improved, as shown in the simulated performance summary in Table 1. On the other hand, the CMRR of the OPAMP with the optimized SC is similar to that of the con-

Fig. 5. Simulated open-loop frequency response of the OPAMPs.

Table 1. Simulated performance of the two-stage OPAMPs.

Items	Conventional OPAMP	OPAMP with SC
Supply voltage	1.8 V	1.8 V
Tail current	20 μ A	20 μ A
DC gain	85.8 dB	99.2 dB
Unity-gain frequency	7.82 MHz	9.85 MHz
Phase margin	60 degree	61 degree
Input-referred noise @1MHz	25.7 nV/(Hz) ^{1/2}	18.9 nV/(Hz) ^{1/2}
CMRR	88.2 dB	85.6 dB
PSRR	115.9 dB	135.0 dB

Load capacitor C_L = 15 pF. Compensation capacitor (C_C) and resistor (R_Z) are 1 pF and 30 k Ω , respectively.

ventional OPAMP, because of the enhanced common-mode gain of the 2nd stage.

3. RESULTS AND DISCUSSION

To confirm the proposed design methodology, the OPAMP with the optimized SC structures, and conventional OPAMP with the single MOSFETs were fabricated, using a 0.18- μ m standard digital CMOS technology. The electrical characteristics of the SC differential input transistors, SC current mirrors, unity-gain buffer using the proposed OPAMP, and finally performance parameters of the fabricated OPAMP were measured.

Figure 6 shows the measured output current (I_{OUT}) and r_{out} characteristics of the current mirror, with the pSC MOSFETs and single pMOSFETs. The overall channel length and width of the MOSFETs were 1.0 μ m and 20.0 μ m, respectively, and the channel length of the source-side MOSFET was 0.6 μ m. The applied bias current was 20 μ A. The semiconductor parameter analyzer (Agilent 4156C) was used for the measurements. The measured r_{out} of the conventional current mirror was 1.1 M Ω at V_{OUT} = 0.9 V, but the measured r_{out} of the pSC current mirror was approximately three times higher than that of the conventional mirror. The enhanced output resistance of the pSC current mirror confirmed the reduced CLM of the MOSFETs.

Figure 7 shows the measured I_{OUT} and r_{out} characteristics of the nSC current mirror. The channel length L_s of the source-side MOSFET was 0.5 μ m, and the channel width of all transistors was 5.0 μ m. The applied bias current was 10 μ A. The measured r_{out} of the conventional current mirror was 1.5 M Ω at V_{OUT} = 0.9 V. On

Fig. 6. Measured r_{out} of the pSC current mirror. V_{DD} and V_{CMP} are 1.8 V and 1.4 V, respectively. The applied bias current is 20 μ A.

Fig. 7. Measured r_{out} of the nSC current mirror. V_{DD} and V_{CMN} are 1.8 V and 0.6 V, respectively. The applied bias current is 10 μ A.

the other hand, the nSC current mirror showed approximately four-fold improvement in r_{out} . The improvement in r_{out} of the nSC current mirror is better than that of the pSC.

Figure 8 shows the measured transconductance generation efficiency (g_m/I_D) of the g_m optimized pSC MOSFETs (L_s = 0.2 μ m) at V_{SD} = 0.9 V. The channel width of all transistors was 20.0 μ m. Compared to the conventional single pMOSFET, the pSC MOS-

Fig. 8. Measured g_m/I_D characteristics of the g_m optimized pSC MOSFET.

Fig. 9. Measured DC transfer characteristics of the unity-gain buffer, using the OPAMP with the optimized SC MOSFETs.

FET showed approximately 30% improvement in the g_m/I_D at a drain current $I_D = 10 \mu\text{A}$.

Figure 9 shows the measured DC transfer characteristics of the unity-gain buffer, using the proposed OPAMP with the optimized SC MOSFETs. The applied input voltage V_{IN} varied from 0 V to 1.8 V. The measured output voltage followed the input voltage over the entire range. The output voltage range of the OPAMP with the optimized SC structures ranged from 80 mV to 1.71 V.

Figure 10 shows the measured large signal step response of the unity-gain buffer using the proposed OPAMP with the optimized SC MOSFETs. The load capacitor C_L was 15 pF. The applied step input voltage and frequency were 1.8 V and 50 kHz, respectively. The maximum rising slew rate of the proposed OPAMP was similar to the ratio of the charging current of MP5 and load capacitor ($\approx I_{MP5}/C_L$) [12]. The rising slew rate of the proposed OPAMP was 1.1 V/ μs , which was a 33% improvement, compared to the conventional OPAMP with the single MOSFETs. Although the charging current of MP5 was identical (20 μA) for both the conventional and proposed OPAMPs, the rising slew rate of the proposed OPAMP could be improved due to the reduced CLM, as shown in Fig. 6.

The DC gains of the fabricated OPAMPs were measured, using

Fig. 10. Measured large signal step response of the unity-gain buffer, using the OPAMP with the optimized SC MOSFETs.

Fig. 11. Micrograph of the proposed OPAMP, with the optimized SC structures.

Table 2. Measured performance of the fabricated OPAMPs.

Items	Conventional OPAMP	OPAMP with SC
Supply voltage	1.8 V	1.8 V
Tail current	20 μA	20 μA
Total power consumption	107.6 μW	108.4 μW
DC gain	70.5 dB	88.0 dB
CMRR	67.5 dB	63.6 dB
Slew rate (rising)	0.8 V/ μs	1.1 V/ μs
Output swing	70 mV–1.78 V	80 mV–1.71 V

a simple measurement technique with a servo loop and auxiliary OPAMP ($\mu\text{A}741$) [13]. The measured DC gain of the OPAMP using the optimized SC was 88.0 dB, which was approximately 18 dB higher than that of the conventional OPAMP. The enhanced g_m and r_{out} of the SC structures resulted in a higher DC gain of the OPAMP. Table 2 lists the measured performance data of the proposed OPAMP, along with that of the optimized SC and the conventional OPAMP.

Figure 11 shows the micrograph of the proposed OPAMP with optimized SC structures, which was fabricated in a standard 0.18- μm triple-well CMOS process. The chip area was 80 $\mu\text{m} \times 86 \mu\text{m}$.

4. CONCLUSIONS

This paper reports a new analog circuit design approach, using SC structures based on the concept of dual-workfunction-gate devices. Both the transconductance and output resistance were influenced by the channel length ratio of the SC MOSFETs. Optimizing the channel length ratio of the SC structure, the highest transconductance and output resistance SC MOSFETs were obtained and utilized in the input differential stages and output stages of the operational amplifier, respectively, to obtain better performance. A two-stage OPAMP using the proposed SC MOSFETs was designed and fabricated. The measured DC gain of the fabricated OPAMP using the proposed SC MOSFETs was approximately 18 dB higher, than that of the conventional OPAMP. The proposed design methodology is a promising solution for low-voltage analog circuit design, particularly in nano-scale CMOS technologies.

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