Electrical Characteristics of Charge Trap Flash Memory with a Composition Modulated $(\text{ZrO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ Film

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This research proposes the use of a composition modulated $(\text{ZrO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ film as a charge trapping layer for charge trap flash memory; this is possible when the Zr (Al) atomic percent is controlled to form a variable bandgap as identified by the valence band offsets and electron energy loss spectrum measurements. Compared to memory devices with uniform compositional $(\text{ZrO}_2)_{0.1}(\text{Al}_2\text{O}_3)_{0.9}$ or a $(\text{ZrO}_2)_{0.92}(\text{Al}_2\text{O}_3)_{0.08}$ trapping layer, the memory device using the composition modulated $(\text{ZrO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ as the charge trapping layer exhibits a larger memory window (6.0 V) at the gate sweeping voltage of ± 8 V, improved data retention, and significantly faster program/erase speed. Improvements of the memory characteristics are attributed to the special energy band alignments resulting from non-uniform distribution of elemental composition. These results indicate that the composition modulated $(\text{ZrO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ film is a promising candidate for future nonvolatile memory device applications.

Keywords: Composition modulated, Atomic layer deposition, Charge trap, Memory

1. INTRODUCTION

With conventional nonvolatile flash memory devices approaching their scaling limitation, tremendous effort has been made to explore the next generation nonvolatile solid state memory devices for use in mobile electronics such as digital cameras, MP3 players, and mobile phones [1-5]. Among the family of nonvolatile memories, the charge trap flash memory (CTFM) is one of the most promising candidates due to its advantages such as better scalability, low power, and process simplicity [6]. Nevertheless, one problem in a conventional CTFM

device with an Si_3N_4 trapping layer is the small potential barrier, which leads to poor retention characteristics. Since the Si_3N_4 based CTFM device faces the challenge of the trade-off between data retention and program/erase speed [7]. In order to further improve memory characteristics and achieve the trade-off among the memory window, program/erase speed and data retention, extensive research has been carried out in recent years. This research has involved the use of nanocrystals (e.g., Ge [8], Si [9], Ni [10], and NiSi [11]), stacked structure [12-14], binary oxide dielectric film (e.g., HfO_2 [15], GdO [16], and ZrO_2 [17]), and multiple oxide dielectric film [18,19] as a charge trapping layer. This work proposes a bandgap engineering technique using a composition modulated $(\text{ZrO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ film as the charge trapping layer in the CTFM device to improve the memory characteristics. This involves the formation of a variable bandgap due to the non-uniform distribution of elemental composition in the charge trapping layer causing different energy band offsets.

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Fig. 2. (a) Valence band spectra and (b) O 1s electron energy loss spectra at the Si surface, TO/Si interface, CM-ZAO/TO interface, from CM-ZAO/TO 3 nm and middle of CM-ZAO.

the above measured positions, respectively. The band gap (E_g) of TO was determined to be 7.3 eV by the onsets of O1s electron energy loss spectra collected at the interfaces of the TO/Si interface, as shown in Fig. 2(b). Similarly, the bandgaps at CM-ZAO/TO, from CM-ZAO/TO 3 nm and the middle of CM-ZAO were 6.0 eV, 5.2 eV, and 4.2 eV, respectively. Therefore, using the formula of $\Delta E_{CBO} = E_g^{Si} - E_g^{TO} - \Delta E_{CBO}$, the calculated value of the conduction band offset (CBO) at TO/Si, CM-ZAO/TO, from CM-ZAO/TO 3 nm and the middle of CM-ZAO were 2.8 eV, 2.0 eV, 1.6 eV, and 1.2 eV, respectively, where is 1.1 eV. According to the composition of the symmetric distribution around the middle of the CM-ZAO film, the energy band alignment of the S1 was schematically depicted in Fig. 3(a). The bandgap of CM-ZAO is determined by the Zr and Al content in the film, which monotonously decreases with increasing Zr content, or increases with decreasing Al content. Therefore, the potential barrier E_B between TO and CM-ZAO (BO and CM-ZAO) is variable and in the range of 0.8 to 1.6 eV. By comparison, the charge-trapping layer has a uniform elemental composition distribution resulting in a changeless potential barrier for S2 and S3, as shown in Fig. 3(b).

Figure 4(a) shows high frequency (1 MHz) C-V hysteresis of S1 with different gate sweeping voltages to observe its charge storage effect. The C-V curves exhibit an obvious memory window (1 V) in a small sweeping range of ± 2 V. When the gate sweeping voltage range is increased to ± 8 V, a significant memory window of 6.0 V can be observed. In addition, the flatband voltage shift (ΔV_{FB}) of the S1, S2, and S3 are shown in Fig. 4(b), in which relatively large ΔV_{FB} are observed under the same gate sweeping voltages for S1, indicating that a tremendous amount of electron

Fig. 3. Schematic energy band alignment of (a) S1, (b) S2 (dotted line), and S3 (dash dotted lines).

Fig. 4. (a) High frequency capacitance-voltage (C-V) curves corresponding to different gate sweeping voltages and (b) ΔV_{FB} extracted from the C-V curves under different gate sweeping voltages. The inset of Fig. 4(a) is the schematic diagram of S1 with Pt patterns to obtain the C-V curves.

Fig. 5. (a) Comparison of the data retention characteristics of S1, S2 and S3 at room temperature. The inset is the energy band alignment of S1 (solid line), S2 (dotted line) and S3 (dash dotted lines), showing the charge loss mechanisms: trapped electrons tunnel from traps to the silicon conduction band (T-B) and thermal excited trapped electrons from the traps to the conduction band followed by tunneling through the tunnel oxide (T-E). The (b) and (d) is the cross sectional TEM images of the S2 and S3, respectively. The SAED patterns (c) and (e) indicate that the $(\text{ZrO}_2)_{0.1}(\text{Al}_2\text{O}_3)_{0.9}$ trapping layer of S2 still maintains an amorphous state, while the $(\text{ZrO}_2)_{0.1}(\text{Al}_2\text{O}_3)_{0.9}$ trapping layer of S3 crystallize, and the diffraction spots correspond to (111), (002), and (113) planes of the cubic ZrO_2 phase, respectively.

traps exist in the charge-trapping layer of S1 compared to the charge-trapping layer of S2 and S3.

We programmed S1, S2, and S3 with an identical initial flatband voltage (6 V) to compare their data retention characteristics at room temperature, as shown in Fig. 5(a). S1 exhibited a slight decrease in flatband voltage, whereas S2 and S3 show obvious charge loss after 1.0×10^5 s, especially for S3. In order to predict the data retention characteristics for a long time, we extrapolated the experimental data for up to 10 years. The results indicate that the decrease in the memory window from the initial 6.0 V to 5.2 V, 4.5 V, and 2.8 V, and the window losses are about 13.3%, 25%, and 53.3% for S1, S2, and S3, respectively. It is known that T-B tunneling and T-E are the important charge loss mechanisms, as shown in inset of Fig. 5(a). At room temperature, the T-B tunneling process is the dominant charge loss mechanism, and can be reduced by increasing the potential barrier E_b [22,23]. Though the charge-trapping layer of S2 is an amorphous state (Fig. 5(b) and (c)), the smaller E_b (0.8 eV) cannot effectively maintain the trapped electrons, which are easily lost via T-B tunneling. Instead, S3 with a maximum E_b (1.6 eV) shows the worst retention performance due to the crystallization of $(\text{ZrO}_2)_{0.92}(\text{Al}_2\text{O}_3)_{0.08}$ charge-trapping layer after post annealing treatment, as shown in Fig. 5(d) and (e). The crystallization of the film will generate grain boundaries, which can act as current leakage paths [18]. The excellent data retention characteristics of S1 should be attributed to the amorphous charge trapping layer [24] and variable potential barrier E_b (0.8 to 1.6 eV), which suppress the leakage of trapped electrons toward the tunneling and blocking oxide.

Figure 6(a) and (b) show the transient program/erase characteristics of S1, S2, and S3 memory devices. The samples are charged at ± 8 V by a single electrical pulse with different width.

Fig. 6. Transient (a) program and erase (b) characteristics of S1, S2, and S3.

It is observed that S1 exhibits a faster program and erase speed than S2 and S3. For example, the program times at a memory window of 1 V for S1, S2, and S3 are 2×10^{-6} s, 2.2×10^{-5} s and 6.8×10^{-4} s, respectively. The results can be explained by the energy band diagram shown in Fig. 3. In a program state, the CBO of CM-ZAO with respect to Si is variable (1.2 to 2.0 eV) in S1, compared to identical CBO 2.0 eV for $(\text{ZrO}_2)_{0.1}(\text{Al}_2\text{O}_3)_{0.9}$ in S2. Hence, at the same gate bias voltages, the electron tunneling distance from the Si substrate to the conduction band of the charge-trapping layer is shorter in CM-ZAO and longer in $(\text{ZrO}_2)_{0.1}(\text{Al}_2\text{O}_3)_{0.9}$. Moreover, the injected electrons are also reduced through blocking oxide into the gate due to the large potential barrier E_b , resulting in a faster program speed for S1 [25]. For the erase case, similar to the program state, the variable VBO (2.9 to 1.9 eV) and large potential barrier result in a faster erase speed for S1 compared to S2. As mentioned above, the poor program and erase speed of S3 should be attributed to the crystallization of the charge-trapping layer.

4. CONCLUSIONS

In summary, a charge trap flash memory with the composition modulated $(\text{ZrO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ charge trapping layer, Al_2O_3 tunneling oxide, and Al_2O_3 blocking oxide has been fabricated and investigated. We have demonstrated that the composition modulated $(\text{ZrO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$ charge trapping layer can simultaneously satisfy a larger memory window, faster program/erase speed, and excellent data retention. The results are attributed to the special en-

ergy band structure of the trapping layer. Based on this work, the charge trap memory device with composition modulated (ZrO_2)_x(Al_2O_3)_{1-x} trapping layer may be a potential candidate for future nonvolatile flash memory device applications.

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