3-D Simulation of Nanoscale SOI n-FinFET at a Gate Length of 8 nm Using ATLAS SILVACO

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Received March 10, 2015; Revised May 21, 2015; Accepted June 5, 2015

In this paper, we present simulation results obtained using SILVACO TCAD tools for a 3-D silicon on insulator (SOI) n-FinFET structure with a gate length of 8 nm at 300K. The effects of variations of the device's key electrical parameters, such as threshold voltage, subthreshold slope, transconductance, drain induced barrier lowering, on-current, leakage current and on/off current ratio are presented and analyzed. We will also describe some simulation results related to the influence of the gate work function variations on the considered structure. These variations have a direct impact on the electrical device characteristics. The results show that the threshold voltage decreases when we reduce the gate metal work function Φ_m . As a consequence, the behavior of the leakage current improves with increased Φ_m . Therefore, the short channel effects in real 3-D FinFET structures can reasonably be controlled and improved by proper adjustment of the gate metal work function.

Keywords: Device scaling, FinFETs, Silicon on insulator, Silvaco software, Work function

1. INTRODUCTION

The trend in miniaturization of electronic components and transistors in integrated circuits has dramatically increased over the past thirty years. The goal is to integrate more components per unit area and, thus, improve circuit performance while lowering their manufacturing cost as predicted by "Moore's Law".

Major semiconductor companies introduced the use of silicon on insulator (SOI) substrate in manufacturing microprocessors to minimize parasitic capacitances and to improve current drive, circuit speed and power consumption [1].

Among the important parameters, which are related to CMOS scaling, the gate length plays a fundamental role. Intel plans to achieve Fin-Shaped Field Effect Transistor (FinFET) technology 10 nm devices in 2015 and 7 nm devices in 2017. Eventually, it will be as low as 1 nm; it will be so small that the quantum physics effects will become relevant [2].

The multi-gate transistors like FinFETs are considered to be the best candidates to extend the use of CMOS technology beyond the barrier of 14 nm. As with classic CMOS technology, the design of integrated circuits requires the availability of high performance and predictive compact models of these devices.

In this work, we study the device structure SOI n-FinFET with an 8 nm gate length by keeping in mind either speed and power consumption as major targets. The region between the source and the drain of the analyzed device is covered by implementing the high-k gate dielectrics (Si_3N_4), which allows further miniaturization of electronic components. In the simulation, the Lom-

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bardi constant voltage and temperature (CVT) and the Shockley-Read-Hall (SRH) models were considered. We also study the influence of variation of the gate work function on the most important parameters, such as threshold voltage (V_{th}), subthreshold slope (SS), transconductance (g_m), drain induced barrier lowering (DIBL), on-current (I_{on}), leakage current (I_{off}), and the on/off current ratio of nanoscale FinFETs.

2. DEVICE STRUCTURE

The schematic structure used for the simulations is represented in Fig. 1. The different parameters of the considered structure are assumed as follows in Table 1:

Table 1. Parameters of symmetrical SOI n-FinFET

Symbol	Designation	Value
L_D, L_S	Drain length and Source length	11 [nm]
L_G	Gate length	8 [nm]
$T_{OX} (Si_3N_4)$	Lateral oxide thickness (gate dielectric material)	1 [nm]
T_{FIN}	Silicon thickness	4 [nm]
H_{FIN}	Fin Height	10 [nm]
$T_{Box} (SiO_2)$	Buried oxide thickness	15 [nm]
$T_{Substrate}$	Substrate thickness	10 [nm]
N_A	Channel concentration	$10^{16} [cm^{-3}]$
N_D	Drain and Source concentration	$10^{20} [cm^{-3}]$

The FinFET technology is based on vertical silicon fin characterized by the fin length (L_G), fin height (H_{FIN}), and the silicon thickness (W_{FIN}) as shown in Fig. 1 [3].

Fig. 1. Illustrates the device structure of an n-FinFET in 3-D with a gate length of 8 nm.

3. 3-D DEVICE SIMULATION USING SILVACO-ATLAS

The software package Silvaco-Atlas was used to construct, examine, and simulate the structure and characteristics of the FinFET device in three dimensions.

In Figs. 2 and 3, I_{DS} - V_{GS} transfer characteristics are shown on a linear scale and log scale for an SOI n-FinFET device structure. In Fig. 2, it is observed that the threshold voltage of an SOI n-FinFET is 0.31 V at $V_{DS} = 0.1$ V. The threshold voltage expression in case of a MultiGate Field-Effect Transistor (MuGFET) device

Fig. 2. I_{DS} - V_{GS} characteristics on a linear scale for an SOI n-FinFET with $\Phi_m = 4.6$ eV at $V_{DS} = 0.1$ V.

structure can be expressed as [1]:

$$V_{Th} = \Phi_{ms} + 2\Phi_f + \frac{Q_D}{C_{ox}} + \frac{Q_{SS}}{C_{ox}} + V_{in} \quad (1)$$

$$\Phi_{ms} = \Phi_m - \Phi_s \quad (2)$$

Where Q_{ss} represents charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, Φ_{ms} represents the metal-semiconductor work function given by the difference between the gate metal work function Φ_m and the semiconductor work function Φ_s , Φ_i is the Fermi potential, which, for P-type silicon, is given by:

$$\Phi_f = \frac{KT}{q} \ln \frac{N_A}{n_i} \quad (3)$$

Where k is the Boltzmann constant, T is the temperature, q is the electron charge, N_A is the acceptor concentration in the p-substrate, and n_i is the intrinsic carrier concentration. The value of KT/q is 0.02586 V at $T = 300$ K.

The transconductance g_m quantifies the drain current variation with a gate-source voltage variation while keeping the drain-source voltage constant [4,5]:

$$g_m = \frac{dI_D}{dV_{GS}} \quad (4)$$

Therefore, the value of g_m is extracted by taking the derivative of the I_{DS} - V_{GS} curve (Fig. 2). The value obtained is 16.14 $\mu A/V$ at $V_{DS} = 0.1$ V.

The threshold voltage (V_{th}) is a very important parameter for obtaining a higher on-state current, which improves the circuit speed. In Fig. 4, it is observed that the on-state current output is 33.26 μA at $V_{GS} = V_{DS} = V_{DD}$ and $V_{DS} = 0.9$ V, where V_{DD} is the supply

Fig. 3. I_{DS} - V_{GS} characteristics on a log scale for an SOI n-FinFET with $\Phi_m = 4.6$ eV at $V_{DS} = 0.1$ V.

Fig. 5. I_{DS} - V_{GS} characteristics for an SOI n-FinFET at different drain voltages with $\Phi_m = 4.6$ eV.

Fig. 4. I_{DS} - V_{GS} characteristics on a log scale for an SOI n-FinFET with $\Phi_m = 4.6$ eV at $V_{DS} = 0.9$ V.

Fig. 6. I_{DS} - V_{DS} characteristics for an SOI n-FinFET at different gate voltages with $\Phi_m = 4.6$ eV.

voltage. Furthermore, I_{DS} is calculated as reported in [4,5]:

$$I_{DS} (nA) = 100 \frac{W}{L} e \frac{q(V_{GS} - V_{Th})}{\eta KT} \quad (5)$$

As the drain voltage is increased, the average velocity of the electrons flowing from the source to the drain increases at a given V_{GS} value. From Fig. 5, it is observed that upon raising the gate voltage above the threshold voltage, the conductance increases. As a result, a larger current will flow when the gate voltage is greater than the threshold voltage and the drain voltage is increased.

The drain current versus drain voltage is plotted in Fig. 6. The effect of the gate voltage on the output characteristics (I_{DS} - V_{DS}) was also observed. The results obtained clearly show a good saturation region of the device at a higher gate bias.

The subthreshold slope (SS) is the major parameter for calculating the leakage current. Furthermore, SS is calculated as in [4,5]:

$$SS (mV/dec) = \frac{d V_{GS}}{d(\log_{10} I_{DS})} \quad (6)$$

A typical value for the SS parameter of a MuGFET is 60 mV/decade, (i.e., a 60 mV change in gate voltage brings about a tenfold change in drain current) [4,5]. The subthreshold slope is 69.13 mV/decade in the considered n-FinFET device at $V_{DS} = 0.1$ V.

The leakage current is directly related to the SS. Fig. 4 shows, that the leakage current output I_{off} is 17.3 pA at $V_{GS} = 0$ V and $V_{DS} = 0.9$ V. I_{off} has been calculated by the following formula in [4,5]:

$$I_{off} (nA) = 100 \frac{W}{L} 10^{\frac{-V_{Th}}{SS}} \quad (7)$$

The leakage current and on-current of the considered device (i.e., 17.3 pA and 33.26 μ A) are improved compared with the results of the recent paper reporting on a 16 nm n-type FinFET

Fig. 7. DIBL effect in an SOI n-FinFET transistor with $\Phi_m = 4.6$ eV.

(i.e., 164 pA and 31.6 μ A) [6]. The lowering of I_{off} is a valuable result in order to minimize the static power dissipation even when the device is in the standby mode. The ratio I_{on}/I_{off} exceeds 10^6 , which indicates the excellent on-state and off-state characteristics.

The value of the drain induced barrier lowering (DIBL) is calculated by using the relation reported in [4, 5]:

$$DIBL (mV/V) = \frac{\Delta V_{TH}}{\Delta V_{DS}} \quad (8)$$

The DIBL is defined as the difference in threshold voltage when the drain voltage is increased from 0.01 V to 0.05 V. In our case, DIBL is 85.30 mV/V for the SOI n-FinFET at a gate length of 8 nm as shown in Fig. 7.

4. EFFECTS OF VARIATIONS OF THE GATE METAL WORK FUNCTION

It is very useful to consider the impact of the gate metal work function Φ_m on the device current and performances. Fig. 8 illustrates the transfer characteristics when Φ_m is increased from 4.5 eV to 4.8 eV in the considered device. We can observe that when the gate work function increases, the threshold voltage increases and the drain current characteristic slope decreases as shown in Figs. 8–10.

In Fig. 11, it is observed that the subthreshold slope does not change with the variation of the gate work function. According to the relationship between I_{off} and V_{th} reported in eq. 7, the threshold voltage increases with a higher metal gate work function, which in turn causes a reduction in the leakage current as shown in Fig. 12.

From Fig. 13, we can notice that the on-current decreases as Φ_m is increased and again, as shown in Fig. 14, the on/off current ratio improves with an increase of Φ_m .

Figure 15 shows that a low value of the gate metal work function leads to a higher g_m value, and a higher drain current as shown in Fig. 13. According to the relationship in eq. 4, g_m is directly related to the drain current (I_d). Therefore, we can conclude that the work function has a very notable effect on the threshold voltage, the transconductance, the leakage current, the on-current and the on/off current ratio.

Fig. 8. I_{DS} - V_{GS} characteristics on a linear scale for an SOI n-FinFET with different values of Φ_m at $V_{DS} = 0.2$ V.

Fig. 9. Threshold voltage versus gate work function of n-FinFET.

Fig. 10. I_{DS} - V_{DS} characteristics for an SOI n-FinFET at different values of Φ_m .

Fig. 11. I_{DS} - V_{GS} characteristics on a log scale for an SOI n-FinFET with different values of Φ_m at $V_{DS} = 0.2$ V.

Fig. 14. On/off current ratio versus gate metal work function.

Fig. 12. Leakage current versus gate metal work function for an n-FinFET.

Fig. 15. Transconductance (g_m) versus gate metal work function.

Fig. 13. On-current variation with different gate metal work function values.

5. CONCLUSIONS

In this work, we have used the numerical simulation tool Atlas Silvaco to construct, examine, and simulate a new SOI n-FinFET with a gate length of 8 nm. As indicated by the three-dimensional simulation results, we found that the short-channel effect (SCE) in SOI n-FinFET can be reasonably controlled and improved by proper adjustment of the metal gate work function. An increased value of Φ_m improves the leakage current and on/off current ratio, but causes a rise of the threshold voltage and a reduction of the device on-current and transconductance as well.

Therefore, this nanometer gate device has shown that it provides improved control of the channel, allowing more efficient reduction of the leakage current at a gate length of 8 nm. We feel confident that the work function will also confirm its strong and positive impact on the electrical device characteristics of multiple-gate MOSFETs to be studied with the same procedure and tool.

REFERENCES

- [1] J. P. Collinge, *FinFET and Other Multi-Gate Transistors* (Springer,

- New York, 2008) p. 339. [DOI: <http://dx.doi.org/10.1007/978-0-387-71752-4>].
- [2] P. Harpe, A. Baschiroto, and K. A. A. Makinwa, *Advances in Analog* (Springer, New York, 2014) p. 418.
 - [3] C. Meinhardt, A. L. Zimpeck, and R. A. L. Reis, *Microelectron. Reliab.*, **54**, 2319 (2014). [DOI: <http://dx.doi.org/10.1016/j.microrel.2014.07.023>].
 - [4] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, *Trans. Electr. Electron. Mater.*, **14**, 291 (2013). [DOI: <http://dx.doi.org/10.4313/TEEM.2013.14.6.291>].
 - [5] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, *Int. J. Adv. Sci. Technol.*, **65**, 19 (2014). [DOI: <http://dx.doi.org/10.14257/ijast.2014.65.02>].
 - [6] W. T. Huang and Y. Li, *Nanoscale Res. Lett.*, **10**, 1 (2015). [DOI: <http://dx.doi.org/10.1186/s11671-015-0739-0>].
 - [7] Z. Arefinia, *Mater. Sci. Semicond. Process.*, **16**, 1240 (2013). [DOI: <http://dx.doi.org/10.1016/j.mssp.2012.11.007>].
 - [8] K. P. Pradhan, S. K. Mohapatra, P. K. Agarwal, P. K. Sahu, D. K. Behera, and J. Mishra, *Microelectron. Solid-State Electron.*, **2**, 1 (2013).
 - [9] M. Zakir Hossain, Md. Alamgir Hossain, Md. Saiful Islam, Md. Mijanur Rahman, and M. Haque Chowdhury, *Global Journals Inc.*, **11**, 7 (2011).
 - [10] E. Bernard, T. Ernst, B. Guillaumot, N. Vulliet, X. Garros, V. Maffini-Alvaro, P. Coronel, T. Skotnicki, and S. Deleonibus, *Solid-State Electron.*, **52**, 1297 (2008). [DOI: <http://dx.doi.org/10.1016/j.sse.2008.04.014>].
 - [11] J. P. Colinge, *Microelectron. Eng.*, **84**, 2071 (2007). [DOI: <http://dx.doi.org/10.1016/j.mee.2007.04.038>].
 - [12] C. Hu, *Modern Semiconductor Devices for Integrated Circuits* (Pearson/Prentice Hall, New Jersey, 2010) p. 351.
 - [13] S. International, *Atlas User's Manual Device Simulation Software* (Silvaco Int., Santa Clara, 2012).