High Performance CMOS Charge Pumps for Phase-locked Loop

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Phase-locked-loops (PLL) have been employed in high-speed data transmission systems like wireless transceivers, disk read/write channels and high-speed interfaces. The majority of the researchers use a charge pump (CP) to obtain high performance from PLLs. This paper presents a review of various CMOS CP schemes that have been implemented for PLLs and the relationship between the CP parameters with PLL performance. The CP architecture is evaluated by its current matching, charge sharing, voltage output range, linearity and power consumption characteristics. This review shows that the CP has significant impact on the quality performance of CP PLLs.

Keywords: CMOS, Charge pump (CP), Phase-locked-loop (PLL), Current mismatch

1. INTRODUCTION

Charge-pump based phase-locked-loops (CPPLLs) are broadly used in various applications especially in modern communication systems [1]. CPPLLs are preferred over other topologies of phase-locked-loops (PLL) due to the advantages of large system gain, low static phase offset and low bias current. Moreover, CP-PLLs ensure the stability of the PLL [2-5].

CPPLLs consist of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), and a voltage-controlled oscillator (VCO) [6-8]. The CP is an essential component of the CPPLL, because it generates the signal and renews the clock pulses at high speeds while integrating the loop filter. In the CP, two switches process the conversion of up and down signals from the PFD into current. The PLL's performance is determined by the PFD and CP optimized to match with zero static phase error. Numerous studies have been carried out to improve CPPLL performance within the PLL system [9-11].

The aim of this article is to study different types of CMOS CPs that have been developed for PLLs. Moreover, the relationship between the CP parameters to the quality performance of PLL is illustrated in this study. This review article is organized as follows. Section II describes the basic concepts of the conventional CP together with CP figure of merits (FOM), the various CMOS CP techniques that have been implemented in PLLs. Section III presents a performance comparison of different types of CP PLL schemes. Finally, conclusions are stated in Section IV.

2. BACKGROUND

The conventional CP is single-ended, consisting of charge and discharge digital output current source, I_{CH} and I_{DIS} respectively as shown in Fig. 1 [12]. Two transistor switches control both digital signals, I_{CH} and I_{DIS} of the PFD. The two switches drive the loop filters and transfer the output signals of the PFD to analogue voltage signals, $V_{CP,OUT}$ to control and charge the capacitance or frequency of the VCO [9].

Theoretically, the charge and discharge of current is equal and matched in an ideal CP, which is converted into voltage in order to tune the voltage controlled oscillator (VCO) via a loop filter [13-15]. However, realistically, the CP introduces non-idealities

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Fig. 1. Conventional charge pump circuit [12].

with static phase error instead of the expected perfect zero phase error. Thus, this non-ideal behavior creates a discrepancy between the CP and PFD, which directly leads the whole PLL system to perform sub-optimally [2,11].

To represent a measure of effectiveness, efficiency and high performance of the PLL a figure of CP merits is required. The PLL figure of merit is the normalized phase noise floor of the phase detector. A CP imperfection can be evaluated by the level of current variation, current mismatch, charge sharing, charge injection and timing mismatch. The mentioned imperfections determine the PLL's reference spur, which is also known as dynamic jitter [7]. The amount of the reference spur, Pr is given by [9,16]:

$$Pr = 20 \log \left(\frac{\Delta\phi f_{BW}}{\sqrt{2} f_{PEF}} \right) - 20 \log \left(\frac{f_{PEF}}{f_{PL}} \right) [dBc] \quad (1)$$

and the loop bandwidth, f_{BW} is given by

$$f_{BW} = I_{CP} R K_{VCO} / (2\pi N) \quad (2)$$

where, $\Delta\phi$ is the phase error, I_{CP} is the current flow in the CP, R is the measured value resistor in the loop filter, K_{VCO} is the gain of VCO, N is the division value, f_{REF} is the reference frequency for the PFD and f_{pl} is the frequency of the pole in the loop filter. The dBc is the unit, which stands for decibel relative to carrier.

Phase error is defined as the error in significant timing and jitter source is in the PLLs using a CP. Reduction of phase error assist precisely controls the PLL dynamics [2,17]. Equation (1) shows that reference spur, Pr is proportional to the phase error, $\Delta\phi$ and loop bandwidth (f_{BW}). Meaning that, reference spurs can be scaled down by decreasing the phase error ($\Delta\phi$) by raising the reference frequency (f_{ref}) or decreasing loop bandwidth (f_{BW}).

The high reference spur (P_r) is also attributed to the great pump current and flat current mismatch [2,9,17]. In addition, the factors of current mismatch, timing mismatch and leakage current lead the imperfection of phase error [3,8,16,18]. The mismatch and leakage current can be represented as:

$$\Delta\phi = 2\pi(\Delta\phi_{leakage} + \Delta\phi_{mismatch} + \Delta\phi_{timing}) \quad (3)$$

where, $\Delta\phi$, $\Delta\phi_{leakage}$, $\Delta\phi_{mismatch}$ and $\Delta\phi_{timing}$ are the phase error, leakage current, current mismatch and timing mismatch of the CP circuit, respectively. The magnitude difference between charging and discharging currents refers to current mismatch [3,8]. In equation (3), current mismatch is directly accompanying the phase error and reference spur. Hence, a CP design is needed that is capable of minimizing the current mismatch and keeps the currents continuous across a wide output voltage range. This is the key to minimize CPPLL phase errors to create an optimum PLL system [2,11,17,19].

Other critical factors that cause current mismatch are charge injection, clock feed and current sharing. Charge injection occurs when the transistor is used to control the switching circuit. PFD output signals and the complementary signals arise when the charge leaks into a capacitive node and the mechanism is turned off [3]. In addition, when current sharing rises from the finite capacitance to the current sources, [20]. Therefore, various methods and designs to reduce current mismatch in CPs is the main target of performance improvement of the PLL, which is described in next section.

2.1 Single ended CMOS CP PLL schemes

Various single-ended CP structures have been proposed in the literature [21-24]. Single-ended CPs are popular as they do not require additional loops and can be classified into three styles according to the switch position, i.e. switch-at-drain, switch-at-gate and switch-at-source [12,14,24].

2.1.1 Basic switch-at-drain and with operational amplifier (Op-Amp) CMOS CP

Figure 2(a) shows the fundamental switch-at-drain CP model while Fig. 2(b) provides the switch-at-drain with operational amplifier. The basic CP switch-at-drain scheme introduces two MOS switches but works sub-optimally [2,4,11]. To overcome the lack of charge sharing, an active operational amplifier was added to switch-at-drain model. With negative feedback amplification, the aim is to obtain a voltage reference equal to voltage output as long as the amplifier remains at high gain. Hence, by ensuring matched currents the voltages at both switches can be sustained

Fig. 2. Switch-at-Drain and amplifier CMOS CP [16].

[24]. The negative feedback amplifier for the CPPLL contributes to the slightly low current mismatch including a decrease in the static phase offset. However, the current mismatch still exists in the basic switch-at-drain and with op-amp CMOS CP described in this section. In addition, the feed-through of the up and down switch signals cannot be proved.

The lack of negative feedback op-amp design is due to the location of the switching transistor connected directly to the output node. Furthermore, because of the modulation effect on the channel length, mismatch between NMOS and PMOS transistors and process variations cause current mismatch [16].

2.1.2 Switch-at-gate CMOS CP

The Switch-at-Gate CMOS CP shown in Fig. 3 demonstrates how the gate is switched as an alternative to the switch-at-drain. The objective is to remove the drawbacks of the switch-at-drain. By this topology, the current mirrors result in a saturation region. The gate capacitance (M1 and M2) and the long channel device are important to implement when the output current of the CP is high. To obtain better matching condition is an advantage. However, the wide and long channel device develops large parasitic capacitance, a consequence of high power consumption and low speed.

Fig. 3. Switch-at-Gate CMOS CP [16].

2.1.3 Basic switch-at-source and with error operational amplifier (Op-Amp) CMOS CP

Another example of CPPLL architecture is when the switch is placed at the source of the current mirror as shown in Fig.4. This basic switch-at-source design maintains M1 and M2 in the saturation region. The switch is linked to the single transistor source with small parasitic capacitance. This topology gives the advantage of a shorter switching time compared to the gate switching design. In addition, the small bias current can be used with huge output current.

Choi, *et al.* described the switch-at-source design with an error operational amplifier (op-amp) addition [25]. The construction of an error op-amp, shown in Fig. 5, is to eliminate the current mismatch in the basic switch-at-source design. This circuit manages to get perfect current matching but the circuit has no clock feed through reduction.

Fig. 4. Basic Switch-at-Source CMOS CP [9].

Fig. 5. Switch-at-Source with Op-Amp CMOS CP [16].

2.2 Dual stage operational amplifier CMOS CP scheme

2.2.1 Rail-to-Rail operational amplifier CMOS CP

Dual stage op-amps are called rail-to-rail op-amp CMOS CP

Fig. 6. Rail-to-rail operational amplifier CMOS CP [9].

structures, consisting of negative feedback and unity gain [9,11]. As shown in Fig. 6 a rail-to-rail operational amplifier, OP₁, is used. The adoption of OP₁ provides a good current match within a wide output of voltage swing. The output voltage of OP₁ accommodates the gate bias voltage, M₅ and M₆, based on the error produced between the V_{OUT} and V_{F1}. Thus, the values of V_{OUT} and V_{F1} are perfectly matched.

In addition, the gain of OP₁ must remain high. The second amplifier of unity-gain, OP₂, is used to support the V_{OUT}, V_{F1} and V_{F2} are identical. Furthermore, the designed gate lengths of all transistors are larger when compared other architecture.

2.2.2 Dual error amplifier CMOS CP

The proposed dual error amplifier CP employs a second compensation circuit or two replica-feedback amplifiers (compensator 1 and 2) with two push-pull charge pumps (CP1 and CP2) as shown in Fig. 7 [7,11]. The function of the first compensator is to control the bias voltage, V_{BP2}, so that the charging current, I_{CH2}, and current of the CP1 are equivalent. The second compensator also controls V_{BN2} to ensure the discharging current I_{DIS2} is equal to the charging current I_{CH1}. This scheme's intention is a low current mismatch.

Fig. 7. Dual error operational amplifier CMOS CP [11].

2.2.3 Rail-to-rail operational amplifier and self-Biasing cascade CMOS CP

Fig. 8. Rail-to-rail operational amplifier and self-biasing cascade CMOS CP [3].

The rail-to-rail operational amplifier and self-biasing cascade, as shown in Fig. 8, is composed of a charge current switch, M₄, which is located in between the V_{DD} and M₅. The discharge current switch, M₁₂, is positioned between ground and M₁₀. The self-biasing current mirror model comprised of the resistor cascade devices ensures that the charge and discharge currents retain an exact value [3,13,26].

On the other hand, the current of I_{UP} is same as the current I₂. The gates of M₅ and M₇ are biased and adjusted by the error amplifier. In this construct, the charge current, I_{up}, matches the discharge current, I_{dw}. In addition, all the transistor gate lengths are also designed to be large enough.

2.2.4 Dual differential amplifier CMOS CP

In the dual differential amplifier CMOS CP scheme, there are different voltage amplifiers to reduce the sensitivity of the pull-up and pushdown currents. Two extra NMOSFETs as shown in Fig. 9 are added in the source branches to create the bias conditions in L₁ and L₂. Thus, the drain-to-source voltage drop, V_{DS}, is matched with MP₂, and MN_{2A}. This includes MN₃, which has similar voltages to V_{DS}.

Fig. 9. Dual differential amplifier CMOS CP [27].

In this scheme, the voltages at nodes B and D are forced to follow nodes A and C, respectively. The area of the gain boosting CP is small compared to passive elements, making it efficient, especially for the capacitors [27].

2.3 Other CMOS charge pump schemes

2.3.1 Differential CMOS CP scheme

Differential CPs have several advantages compared to single-ended ones. They are preferred to single-ended CPs in high-performance applications due to their immunity to common-mode noise and power supply variation [18,28]. Differential CPs are composed of two loop filters and a common-mode feedback circuit, as shown in Fig.10. Hence, its structure requires a large area to create extra power dissipation.

The differential amplifier is built of two current sources (NMOS and PMOS) and four switches [18,29]. In this architecture, the output of the transmission gate is connected to the loop filter. This is in addition switches the CP output current.

The two extra switches, which are toggled by the inverters (INV1 and INV2), provide a dual current flow path. When both the signals are in a high state, the current flow through transistors MP20 and MN22 move up and down. However, when both signals are in the low state, the current flows via MP17 and MN19 transistors. An amplifier of A1 is included in this structure to eliminate the impact of parasitic switches capacitance.

Fig. 10. Differential CMOS CP.

2.3.2 Three Rail-to-Rail Operational Amplifier CMOS CP

A three rail-to-rail operational amplifier often known as a compensated CP for PLL is presented in Fig. 11 [19]. The CP uses two regulation loops. One is the current source consisting of M3 and M4, the other focuses on current sink, consisting of M5, M6 and M7. The amplifier of OP₁, applied in dual stage op-amp, which is included in this three rail-to-rail operational amplifier design [9]. This is due to transistor mismatch to compensate by equalizing the drain with the output of the switched current by controlling the current mirror gate bias.

However, this architecture develops new mismatch source, which is the difference between the drain potentials and the input branch. Hence, amplifier OP₃ is used to match all the expected possibility. Amplifier OP₂ will buffer the output voltage of the CP. This design will also regulate both source and sink currents of the CP; therefore, the need of the output potential absolute current parameter will reduce.

Fig. 11. Three rail-to-rail operational amplifier CMOS CP [9].

2.3.3 D-flip-flop CMOS CP

In this structure, D flip-flop CMOS CP is comprised of two D flip-flops, reset, AND gate, NOT gate, and a delay cell. After passing via the unit of NOT gate block and delay, two output signals of D flip-flop will rebound by re-setting the end of the D flip-flop [20].

The D flip-flop CMOS CP circuit is made up of transistors as shown in Fig. 12 form the current mirror in order to obtain a charging and discharging current for the low pass filter. In addition, the transistor also builds the switching circuit to adjust the

Fig. 12. D-flip-flops CMOS CP [20].

output and complementary signals. The four groups of switches manage to reduce the charge injection and clock feed through. The single amplifier protects the voltage at node A and B causing them to be constantly equal with the output voltage. This is to ensure and to avoid voltage bouncing due to charge sharing.

2.3.4 New source-switching CP with op-amp and current reference

Source-switching CP with op-amp and current reference was proposed by Zhou and Wang [28]. The architecture presents the charge current, I_{UP} and the discharge current, I_{DN} . Both the I_{UP} and I_{DN} develop via the current mirrors from the same reference current source of 200 μ A. In addition, a high-gain operational amplifier, as shown in Fig. 13, is also included in the CP to ensure the voltage V_{REF} is perfectly matched to the voltage V_C . However, the matching is only achievable if the gain of amplifier is maintained properly.

This design is composed with typical supply-independent current reference to provide current bias in the whole CP system. In addition, the current reference, I_{REF} uses only 50 μ A to recover and save power consumption in the CP.

The proposed design is comprised of an amplifier but has small voltage gain, relatively corresponding to 76 dB. Thus, due to the small voltage gain, the current mirror effect can be ignored and perfect current matching obtained.

Fig. 13. Source-switching CP with Op-amp and current reference [28].

2.3.5 Gain boosting charge pump for PLL

Li, *et al.* designed the gain-boosting circuit scheme for CP [6]. Fig. 14 shows that the CP, MP₄, and MN₄, are the current sources for the single-transistor amplifiers. The output resistance, labeled MN₁ and MP₁, are used to deliver a gain-boosting circuit. This condition upgrades the output resistance of the CP, which enhances and improves the current matching characteristics.

The trans-conductance and output resistance of the nMOS

The techniques negative feedback and dual negative feedback op-amp is proposed to manage and to reduce the current mis-

Table 1. Performance comparison of various single-ended CMOS CP schemes for PLL.

Year Published [Ref. No.]	Process Architecture	CMOS Process (μm)	Voltage Supply (V)	Current Variation	Current mismatch (mA)	Static Phase Offset (sec)	Reference Spur (dBc)	Power (mW)
2009 [31]	switch-at-drain with negative feedback amplifier	0.65	1.8	< 2%	-2.2 to 1.8 mA	-25ps to 7ps	-70	65.00
2004 [33]	switch-at-drain with negative feedback amplifier	0.18	1.8	< 2.0%	-2.0 to 2.1	-	-65	99.00
2004 [35]	switch-at-drain with negative feedback amplifier	0.9	1.0	-	0.125 to 0.875	-	-	48.00
2003 [23]	switch-at-drain with negative feedback amplifier	0.18	1.8	-	-	-	-65	302
2000 [32]	switch-at-source with an error amplifier	0.25	2.5	< 2%	0.1 to 1.2	-	-75	7.00
2006 [34]	switch-at-source with an error amplifier	0.13	1.2	-	-	-	-54	10.00
2000 [25]	switch-at-source with an error amplifier	0.25	1.2	< 1%	0.1 to 1.1	-	-75	12.00
2014 [22]	switch-at-gate	0.65	0.4	-	-	30.8	-55.3	109
2010 [36]	Differential Amplifier	0.18	1.8	< 2%	-0.05 mA to mA	-	-80	8.87
2013 [21]	OTA	0.18	1.8	< 1.8%	1 mA to 8.5 mA	-	-73	5.14

Table 2. Performance comparison among various schemes of dual stage op-amp CMOS CP.

Year Published [Ref. No.]	Process Architecture	CMOS Process (μm)	Voltage Supply (V)	Current Variation	Current mismatch	Reference Spur (dBc)	Power (mW)
2007 [9]	negative feedback and unity gain op-amp	0.18	1.8	1.5%	< 0.5%	- 60.1	0.57
2009 [11]	dual negative feedback op-amp	0.13	1.2	1.7%	< 3.2%	- 63.7	1.8
2007 [26]	replica biasing and feedback	0.18	1.2	-	< 0.5 %	-	0.85
2012 [13]	op-amp and biasing cascode	0.18	1.8	-	< 0.4%	-	0.9
2013 [27]	dual differential op-amp	0.18	1.8	-	< 0.1%	-	-
2010 [7]	dual feedback op-amp	0.13	1.2	-	< 0.6%	-56	2.1

match significantly and align with wide current variation, but increase circuit complexity [9,11]. The constructions of larger transistors lead to a fast switching operation that allows disadvantages.

Expanding the input of rail-to-rail operational amplifier and the self-biasing cascade current mirror method enable the current of CP circuit, which is matched in a large range output voltage. Additionally, a proposed method of adding a pre-charging current source to raise the initial charge current and enhance the speed up of the CPPLL settling time. Extra consideration and stable analysis should apply to this connection as the composition simultaneously delivers a positive and negative feedback loop. In addition, the implementation of cascade current mirrors tends to reduce the voltage headroom.

The design of dual differential amplifiers based on a switches-in-source construction improved through gain-boosting amplifiers for CPPLLs. Two differential amplifiers were employed in dual differential amplifier CPs to reduce the channel length modulation effect in MOS transistors. This is an advantage to the current up and down more towards independent of the output voltage. Nevertheless, the design is only verified by simulations. Table 2 shows the performance comparison among various schemes of dual stage op-amp CMOS CP.

In addition, the method of dual stage op-amps in three rail-to-rail amplifiers is capable and proven to match the drain with the output of the switched current by adjusting the current mirror gate bias. This significantly reduces the current mismatch. However, the major concern in this design is the strength of control loops. This concern was investigated and analyses only involve in simulation. The simulation suggests a design using short-channel devices with high voltage supply.

The design of the D flip-flop CMOS CP provides the advantages of low-power, low-jitter and high speed. The mixed architecture of digital and analog techniques contributes high precision and strength, including a high performance amplifier for CPPLLs. The D-flip-flops are included in this structure to defeat the dead phase-zone and current mirrors. The major aim of the D flip-flop CMOS CP development is to apply it in the high certainty of inertial sensors.

The gain-boosting circuit improves current matching characteristics together with the reduction of the channel-length modulation effect. Advantages of this gain boosting CP are current mismatching characteristics are achieved without the need of stacking extra cascade devices, operational amplifiers, a feedback circuit, a complicated replica CP, and an additional compensation CP. In addition, the gain-boosting CP circuit is suitable for a low power supply voltage.

The design of differential CPs and operational trans-conductance amplifiers show that both methods are able to reduce current mismatch but the variation of the current still remains. Apart from that, differential CPs are frequently used for applications in high-speed and high-performance PLLs. All schemes produced high power consumption [25,31]. Thus, a differential charge pump needs to be avoided to limit power dissipation. Table 3 shows the performance comparison among different schemes to design a suitable CP for PLL.

Table 1 suggests several research methods for designing a high performance single-ended CP circuit for PLLs. However, some design schemes consume more power compared to others. It is obvious that OTA [21] topology requires the lowest power dissipation compared to other mentioned topologies. None of the design schemes with single-ended CMOS CP circuits are able to

Table 3. Performance comparison among various schemes of other CMOS CPs.

Year [Ref. No.]	Process Architecture	CMOS Process (μm)	Voltage Supply (V)	Current mismatch	Jitter (ps)	Power (mW)
2014 [19]	three rail-to-rail op-amp	1.8	3	< 2.1%	-	-
2011 [20]	D flip-flop CMOS CP	-	4	< 1.0%	931.32	6.3
2008 [28]	New source-switching CP with op-Amp and current reference	0.18	1.8	< 1.62%	-	958.5
2006 [6]	Gain boosting	0.18	1.8	< 1.2%	-	-
2006 [37]	Adaptive bandwidth PLL	0.09	1	-	4 (with CP)	3.252
2007 [38]	Op-amp	1.8	1.8	< 2%	-	6.84
2011 [39]	rail-to-rail operational amplifier	1.8	1.8	< 0.5	-	0.57

provide a perfect current match or zero average current.

On the other hand, Table 2 illustrates various dual stage op-amp CMOS CP circuits. Table 2 compares single stage designs and exhibits how dual stage designs are able to reduce the power dissipation. In addition, some of the designs are also able to reduce current mismatch. Due to these current mismatches, some offset values are present in these designs.

Conversely, Table 3 gives a summary of different design methods with different output parameters for CPs. PLL performance depends mainly on the CP output parameters. Therefore, all the parametric values like jitter, reference spur, power dissipation and current mismatch should be taken into consideration during CP circuit design.

In addition, phase offset, which raises the spur in PLL directly, is connected with some parameters of CP such as, perfect current match, zero average current and zero net charge. Nevertheless, from Table 1, Table 2 and Table 3 we observed that, none of the design topologies is able to provide a perfect current match.

4. CONCLUSIONS

This review article has discussed the present research on CMOS CP for PLL. From the research presented, we conclude that even though there are various schemes of CP which have been implemented for PLLs, the selection of the CPs is based on the PLL applications and the complexity of the scheme. The CP output parameters are the main impact on PLL performance. CP based PLLs need a perfect current match, zero average current and zero net charge because it has significant impact on the phase offset, which increases spur in PLL. The phase offset could reduce the locking range and degrade PLL performance.

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