Conducted-Noise Characteristics of a Digitally-Controlled Randomly-Switched DC-DC Converter with an FPGA-Based Implementation

Gamal M. Dousoky[†], Masahito Shoyama*, and Tamotsu Ninomiya**

[†]* Graduate School of Information Science and Electrical Engineering, Kyushu University, Japan

** Faculty of Engineering, Nagasaki University, Japan

Abstract

This paper investigates the conducted-noise characteristics of a digitally-controlled randomly-switched dc-dc converter. In order to investigate the effect of the suggested digital controller on the conducted-noise characteristics of a dc-dc converter, three factors have been studied: the field-programmable gate array (FPGA) clock speed, the randomization ratio percentage, and the effect of using a closed loop feedback controller. A field-programmable gate array is much more flexible than analog control circuits, has a lower cost, and can be used for power supply applications. A novel FPGA-based implementation has been suggested for obtaining the experimental validations and realizing the studied concepts. Furthermore, the experimental results have been discussed and design guidelines have been included.

Key Words: DC-DC converter, Electromagnetic compatibility, Electromagnetic interference, Field programmable gate arrays, Random number generation

I. INTRODUCTION

Power electronics have become the dominant factor in the deterioration of our electromagnetic environment, causing a decline in line power and an increase in the level of conducted electromagnetic interference (EMI) [1].

In general, semiconductor switches produce differential-mode conducted EMI through the basic power-conversion process and common-mode conducted EMI through capacitive or inductive coupling [1], [2].

Recent electromagnetic compatibility (EMC) regulations recognize the need for reducing the harmonic pollution of power lines, and limit the amount of harmonic current emissions [3]–[5].

Traditional solutions are related to filters and shielding techniques. However, these solutions have a number of limitations and drawbacks, which prevent universal applicability. Alternatively, random-switching techniques attenuate the switching noise by spreading them over a frequency range. This is typically achieved by randomly varying the switching frequency of the switching power supplies. Random-switching control is effective for suppressing the peak level of the switching-noise spectrum [2], [6]–[20]. Furthermore, the effects of randomizing the duty cycle and some other randomization techniques

on the switching noise characteristics have been addressed in several publications [10], [11].

Hardware limitations and the complexity of the control circuits cause difficulty in achieving compliance with standard EMC regulations while maintaining low conducted EMI and low cost. On the other hand, with the flexibility and programmability of FPGA technology, many attractive techniques can be designed and implemented as well [21]–[22]. The implementation of the proposed controller has been accomplished using FPGA technology.

Electromagnetic interference mitigation in a switching-mode power supply (SMPS) is a very active research topic, yet there is a lack of meaningful analyses and design guidelines especially in case of digital control.

This paper is organized as follows: Section II describes a randomly switched dc-dc converter using FPGA. Section III presents the details of the experimental work setup. Experimental results and analysis are presented in section IV. Finally, the conclusions are presented in section V.

II. RANDOMLY SWITCHED DC-DC CONVERTER USING FPGA

Fig. 1 illustrates the overall circuit block diagram of a randomly switched dc-dc converter using an FPGA. It consists of a dc-dc power switching circuit, an analog to digital conversion circuit and its driver, the proposed FPGA-based digital controller, and interface and power switches and their drivers.

Manuscript received Oct. 22, 2009; revised Mar. 31, 2010

[†] Corresponding Author: dousoky@ieee.org

Tel: +81-92-802-3704, Fax: +81-92-802-3703, Kyushu University

* Graduate School of Information Science and Electrical Engineering, Kyushu University, Japan

** Faculty of Engineering, Nagasaki University, Japan

Fig. 1. Block diagram of a randomly switched dc-dc converter using FPGA-based digital controller.

Fig. 2. Flowchart of the designed digital compensator.

A. Converter Power-Circuit Design

A synchronous buck converter topology has been selected in order to improve efficiency and reduce heat loss [23]. The sizes of the output inductor and capacitor have been chosen such that:

- The converter operates in continuous conduction mode (CCM) at minimum output current.
- The peak-to-peak value of ripple voltage is within $V_r = 20$ mV.
- Current ripple ratio $r \approx 0.4$.

B. Analog to Digital Conversion Circuit and Its Driver

The converter output voltage is converted into a digital 8-bit signal by means of an analog to digital converter (ADC). This signal is processed by the digital compensator to calculate the duty ratio (d). The ADC's driver is designed and embedded inside the FPGA-based digital controller. The conversion cycle is started with the switching cycle and completed within the same switching cycle.

C. Digital Compensator

In order to regulate the output voltage to match a precise voltage reference over a range of input voltage values, load currents, and temperature variations, a digital compensator has been designed. Moreover, the digital compensator makes the output voltage immune to randomized variations in the

Fig. 3. The proposed pseudorandom stream generator.

switching frequency. Fig. 2 illustrates the operation of the proposed FPGA-based controller.

During the current switching cycle, the digital compensator computes the digital duty ratio ($d(n+1)$ for the next switching cycle) in one of three modes. These modes can be explained as follows:

Step Decrease Mode: when the output voltage is higher than the upper threshold voltage ($V_{ref} + d_z$), the duty ratio is reduced by a step change (Δd).

Step Increase Mode: when the output voltage is less than the lower threshold voltage ($V_{ref} - d_z$), the duty ratio is increased by a step change (Δd).

Deadzone Mode: when the output voltage lies between the threshold voltage limits $\{(V_{ref} - d_z), (V_{ref} + d_z)\}$, approaching the desired reference value, the duty ratio is frozen.

In this way, the use of a deadzone comparator prevents undesired oscillations in the converter output. Thus, a stable operating condition is obtained.

D. Pseudorandom Stream Generator

A pseudorandom stream generator has been constructed as shown in Fig. 3. The proposed construction uses several maximum length linear feedback shift registers (m-LFSRs) in parallel. The use of m-LFSRs is due to the fact that the sequence generated by the m-LFSRs has a maximum period [24]. For different m-LFSRs output bits, different initial contents of the m-LFSRs (seeds) have been used. The taps are XOR'd sequentially with the output and then fed back into the leftmost bit.

The designed pseudorandom stream generator delivers a 16-bit output; (the maximal number is $2^{16} - 1 = 65535$). The random stream is composed of the output bits of the

Fig. 4. Gate signal generation with the digital pulse width modulator, (DT denotes the dead time).

Fig. 5. VHDL simulation of the proposed FPGA-based digital controller.

component m-LFSRs. The component m-LFSRs are clocked regularly; i.e., the movement of the data in all of the m-LFSRs is controlled by the same clock.

At the beginning of every switching cycle, the random output bits are converted into an integer number (PRN) and used in the digital pulse-width modulator (DPWM). However, the other generated random output bits are discarded.

E. Digital Pulse Width Modulator

At the beginning of every switching cycle, the DPWM achieves the following assignments:

- 1) Taking $d(n+1)$ as input and considering it as the duty ratio of the started switching cycle ($d(n)$).
- 2) Converting the pseudorandom output bits into an integer number (PRN).
- 3) Calculating the needed number of clocks (SN and DN) to fulfill the switching frequency and duty ratio, respectively, for the started switching cycle, as follows:

$$f_{sw} = f_L + K \times PRN \quad (1)$$

$$SN = f_{clk} / f_{sw} \quad (2)$$

$$DN = SN \times d(n) \quad (3)$$

Fig. 6. Measured efficiency of the designed converter (at $V_{in} = 12$ V and $d = 0.3$).

Fig. 7. The effect of using the proposed controller on the converter output characteristics, (at $V_{in} = 12$ V, $I_o = 5$ A, and $d = 0.3$).

where;

f_{sw} : Switching frequency

f_L : Lower frequency limit

K : Constant for achieving the required randomized frequency range

PRN : Pseudorandom output stream converted into an integer number

SN : Needed number of steps to fulfill the switching frequency

f_{clk} : Clock frequency

DN : Needed number of steps to fulfill the duty-ratio

As shown in Fig. 4, the designed DPWM uses a clocked-counter that increments (up to SN) and resets at the end of the switching cycle (see the $reset1$ signal in Fig. 5). When the counter value exceeds the reference value (DN), the PWM output changes its state from high to low. In this way, the digital pulse-width modulated waveforms ($V_{gs1,2}$) with the commanded duty ratio at the calculated switching frequency are generated.

Fig. 8. The experimental circuit for conducted-noise measurements.

Fig. 9. The effect of FPGA clock speed on the noise level reduction.

Fig. 11. The effect of randomization ratio percentage on the noise level reduction.

Fig. 10. The effect of increasing the FPGA clock speed on the randomization resolution, (for output signal with randomized frequency range 270~330 kHz).

III. EXPERIMENTAL WORK

The randomly switched dc-dc converter, described in section II, has been designed and implemented using an Altera FPGA. The VHDL simulation of the proposed FPGA-based controller is shown in Fig. 5. Table I illustrates the synchronous buck

Fig. 12. Frequency variation's normalized probability mass function.

converter parameters.

The measured efficiency of the converter at different switching frequencies is shown in Fig. 6. Basically, the higher the switching frequency the higher the switching losses, thus the lower the efficiency. It is clear that the upper curve (at $f_{sw} = 100$ kHz) has different characteristics at a low output current (at $I_o < 3$ A). This can be attributed to the fact that: at this range of switching frequency and output current, the converter enters the discontinuous conduction mode (DCM) of operation.

Moreover, the effect of using the proposed controller on the converter output characteristics is illustrated in Fig. 7. It is clear that the output voltage is well regulated using the

TABLE I
THE SYNCHRONOUS BUCK CONVERTER PARAMETERS

Symbol	Description	Value
V_{in}	Input voltage (V)	12
V_o	Output voltage (V)	3.3
I_o	Output current (A)	5
f_{csw}	Center switching frequency (kHz)	300
L	Output inductor (μ H)	4.3
C	Output capacitor (μ F)	470
C_{in}	Input capacitor (μ F)	100

proposed controller.

The conducted-noise has been measured across the input terminals of the converter using a line impedance stabilization network (LISN) [3]. Fig. 8 describes the experimental circuit for conducted noise measurements. The LISN is used to standardize the input impedance from the converter input and to sense the conducted-noise, which is measured by an EMI receiver. The resolution band width of the spectrum analyzer has been adjusted to (RBW = 9 kHz).

In order to investigate the effect of random-switching on the conducted-noise characteristics of the dc-dc converter using an FPGA, three factors have been studied as follows:

- 1) FPGA clock speed, (20 MHz, 40 MHz, and 66 MHz speeds have been used).
- 2) Randomization ratio percentage, (*RRP*):

$$RRP = \frac{K * PRN}{2 * f_{csw}} * 100 \quad (4)$$

where;

RRP : Randomization ratio percentage,

f_{csw} : Center switching frequency.

- 3) Using the feedback controller (FB) or using a fixed duty-ratio (Fixed d).

IV. RESULTS AND ANALYSIS

A. FPGA Clock Speed Effect

As illustrated in Fig. 9, the noise level reduction increases when using a higher FPGA clock speed, since the randomization resolution increases. This can be explained as follows:

Any output signal from the FPGA is composed of a number of clocks. Then, the frequency of this output signal can be calculated with the following equation:

$$F_{output\ signal} = \frac{1}{clocks\ No. * T_{clk}} = \frac{f_{clk}}{clocks\ No.} \quad (5)$$

where;

$F_{output\ signal}$: Frequency of the output signal

T_{clk} : Time period of each clock cycle = $1/f_{clk}$

From the above equation, for an output signal with a certain frequency randomization range, a higher FPGA clock speed permits a wider range of clock numbers (i.e. a larger number of different candidate frequencies), which means a higher randomization resolution as illustrated in Fig. 10. On the other hand, the higher FPGA clock speed, the higher the FPGA cost.

Fig. 13. Overlapping between the successive frequency spectrum ranges.

Fig. 14. The effect of using the feedback controller on the noise level reduction (at $f_{clk} = 66$ MHz).

B. Randomization Ratio Percentage Effect

The results, shown in Fig. 11, reveal that increasing the randomization ratio increases the noise level reduction until a certain ratio where the noise level reduction again decreases. The latter is due to the increased low-frequency noise and the overlaps between the successive frequency spectrum ranges in the case of higher randomization ratios that can be clarified as follows:

Assuming a random pulse train with a uniform frequency distribution at a constant duty ratio, as shown in Fig. 12, the switching frequency changes uniformly from f_L up to f_H in

Fig. 15. Comparison between the spectrum of the conducted-noise of the buck converter with fixed switching frequency (0% RRP) and that with randomized switching frequency (21.8% RRP), (at $f_{clk} = 66$ MHz, using the FPGA feedback controller, and at RBW = 9 kHz).

the range of $f_{csw} \pm \Delta f$.

As illustrated in Fig. 13a, at zero Δf i.e. fixed switching frequency PWM, the frequency spectrum of the pulse train will be concentrated at the switching frequency and its multiples.

Slightly increasing Δf as random PWM spreads the frequency spectrum of the signal decreases the spectrum's peaks as in Fig. 13b. However, large values of Δf cause overlapping between the successive frequency spectrum ranges that increases the frequency spectrum envelope which in turn increases the low-frequency components. In addition, it also generates superposed peaks with higher values than those generated using a low Δf , as shown in Fig. 13c. To avoid such overlapping, the boundaries of the switching frequency variation should fulfill the following constraint:

$$f_H \leq 2f_L \quad (6)$$

substitute with:

$$\begin{aligned} f_L &= f_{csw} - \Delta f, \quad \text{and} \\ f_H &= f_{csw} + \Delta f, \end{aligned}$$

then,

$$\begin{aligned} f_{csw} + \Delta f &\leq 2(f_{csw} - \Delta f) \\ 3\Delta f &\leq f_{csw} \end{aligned}$$

thus,

$$\Delta f / f_{csw} \leq 1/3. \quad (7)$$

That means $\Delta f \leq 33.33\%$ of f_{csw} which strongly agrees with the experimental results shown in Fig. 11.

C. Effect of Using the Feedback Controller

Fig. 14 shows the effect of using the feedback controller on noise level reduction. It is clear that, the feedback controller effectively regulates the output voltage. However, it slightly decreases the noise level reduction.

Changing the switching frequency (i.e. changing the switching time from cycle to cycle); digitally: changing the number

of clocks SN and in turn the DN produces quantization problems that induce a ripple in the output voltage.

On the other hand, the feedback digital controller tries to keep the output voltage at a desired reference value without any deviations. To achieve this, the controller alters the duty cycle. These oscillations deteriorate the noise spectrum-spreading achieved by random switching.

Finally, the comparison, shown in Fig. 15, reveals that the conducted-noise spectrum has been significantly improved and that the noise level has been effectively reduced. Table II illustrates a summary of the achieved noise level reductions for the studied cases.

TABLE II
SUMMARY OF THE ACHIEVED NOISE LEVEL REDUCTION FOR THE STUDIED CASES(dB).

RRP, %	$f_{clk} = 66$ MHz		$f_{clk} = 40$ MHz		$f_{clk} = 20$ MHz	
	Fixed d	FB	Fixed d	FB	Fixed d	FB
10.922	9	8.6	7	8.6	4.6	3
21.845	9.6	8.8	8.6	8.4	7.4	5
32.768	9	7.2	7.6	9	8	7
43.69	7.6	7.8	4.6	7.2	5	5.8
54.613	5.2	5.8	3.6	5.8	1.8	3.4
65.535	5	5.6	2.2	4	1.4	3

V. CONCLUSIONS

A novel FPGA-based controller has been designed and implemented for conducted-noise reduction in dc-dc converters. Moreover, the conducted-noise characteristics of a digitally-controlled randomly-switched dc-dc converter have been experimentally investigated. It can be concluded that:

- 1) Increasing the FPGA clock speed improves the conducted-noise spectrum of the converter. On the other hand, the higher FPGA clock speed, the higher the FPGA cost.

- 2) The feedback controller effectively regulates the output voltage. However, it slightly attenuates the noise reduction.
- 3) Increasing the randomization ratio increases the noise reduction until a certain ratio where the noise reduction again decreases. The latter is due to the increased low-frequency noise and the overlaps between the successive frequency spectrum ranges. To avoid such overlapping, a randomization ratio shouldn't be taken that is more than $\pm$ one third of the central switching frequency.

Finally, experimental results show that, using the proposed FPGA-based controller significantly improves the converter's EMI performance.

REFERENCES

- [1] R. Redl, "Power electronics and electromagnetic compatibility," in *Proceeding of IEEE Power Electronics Specialists Conf.*, Vol. 1, pp. 15-21, 1996.
- [2] T. Tanaka, T. Ninomiya, and K. Harada, "Random-Switching Control in DC-to-DC Converters," in *Proc. IEEE Power Electronics Specialists Conf.*, Vol. 1, pp. 500-507, 1989.
- [3] R. Paul, *Introduction to Electromagnetic Compatibility*, John Wiley & Sons, 2nd ed., pp. 49-90, 2006.
- [4] C. Christopoulos, *Principles and Techniques of Electromagnetic Compatibility*, CRC Press, 2nd ed., chap. 13, 2007.
- [5] T. Williams, *EMC for Product Designers*, Elsevier Press, 4th ed., chap. 4-5, 2007.
- [6] T. Ninomiya et al., "Noise Reduction of Switching-Mode Power Converters by Random-switching Control," in *Proc. IPEC-Tokyo'90*, pp. 1165-1172, 1990.
- [7] T. Tanaka, H. Kameda, and T. Ninomiya, "Noise Analysis of DC-to-DC Converter with Random-switching Control," in *Proc. IEEE INT-ELEC'91*, pp. 283-290, 1991.
- [8] A. M. Stankovic, G. C. Verghese, and D. J. Perreault, "Analysis and Synthesis of Randomized Modulation Schemes for Power Converters," *IEEE Trans. Power Electron.*, Vol. 10, pp. 680-693, Nov. 1995.
- [9] T. Tanaka, H. Hamasaki, and H. Yoshida, "Random-Switching Control in DC-to-DC Converters: An Implementation Using M-sequence," in *Proc. IEEE INTELEC'97*, pp. 431-437, 1997.
- [10] K. K. Tse et al., "A Comparative Investigation on the Use of Random Modulation Schemes for DC/DC Converters," *IEEE Trans. Ind. Electron.*, Vol. 47, No. 2, pp. 253-263, Apr. 2000.
- [11] F. Mihalic and D. Kos, "Reduced Conductive EMI in Switched-Mode DC-DC Power Converters without EMI Filters: PWM Versus Randomized PWM," *IEEE Trans. Power Electron.*, Vol. 21, No. 6, pp. 1783-1794, Nov. 2006.
- [12] G. M. Dousoky, M. Shoyama, and T. Ninomiya, "FPGA-Based Design and Implementation of Spread-Spectrum Schemes for Conducted-Noise Reduction in DC-DC Converters," in *Proc. IEEE-ICIT09*, pp. 527-532, 2009.
- [13] —, "Studying the Design and Performance of Conducted-Noise Spectrum Spreading in DC-DC Converters with an FPGA-Based Controller," in *Proc. EMC'09/Kyoto*, pp. 229-232, Jul. 2009.
- [14] —, "Triple-Hybrid Spread-Spectrum Technique for Conducted-Noise Reduction in DC-DC Converters with an FPGA-Based Implementation," in *Proc. EPE 2009*, pp. 1-8, Sep. 2009.
- [15] J. Chai et al., "On Acoustic-Noise-Reduction Control Using Random Switching Technique for Switch-Mode Rectifiers in PMSM Drive," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 3, pp. 1295-1309, Mar. 2008.
- [16] S. Kaboli, J. Mahdavi, and A. Agah, "Application of Random PWM Technique for Reducing the Conducted Electromagnetic Emissions in Active Filters," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 4, pp. 2333-2343, Aug. 2007.
- [17] D. Gonzalez et al., "Conducted EMI Reduction in Power Converters by Means of Periodic Switching Frequency Modulation," *IEEE Trans. Power Electron.*, Vol. 22, No. 6, pp. 2271-2281, Nov. 2007.
- [18] R. Yang et al., "Time-Frequency and Wavelet Transforms of EMI Dynamic Spectrum in Chaotic Converter," *IEEE Trans. Power Electron.*, Vol. 24, No. 4, pp. 1083-1092, Apr. 2009.
- [19] S. Kim, W. Choi, S. Choi, and K. Lee, "Combined Dithered Sigma-Delta Modulation based Random PWM Switching Scheme," *Journal of Power Electronics*, Vol. 9, No. 5, pp. 667-678, Sep. 2009.
- [20] M. Nguyen, Y. Jung, H. Yang, and Y. Lim, "Harmonic Intensity Reduction Technique for Single Phase Switched Reluctance Motor Drives Using a New Random PWM Scheme," *Journal of Power Electronics*, Vol. 10, No. 1, pp. 51-57, Jan. 2010.
- [21] "What Is the Next Implementation Fabric?," *IEEE Design & Test of Computers*, Vol. 20, No. 6, pp. 86-95, Nov/Dec. 2003.
- [22] T. Yokoyama, N. Doi, and T. Ishioka, "Verification of an Autonomous Decentralized UPS System with Fast Transient Response Using a FPGA-Based Hardware Controller," *Journal of Power Electronics*, Vol. 9, No. 3, pp. 507-515, May 2009.
- [23] Miftakhutdinov and J. Zbib, "Synchronous Buck Converter with Increased Efficiency," in *Proc. IEEE Applied Power Electronics Conf.*, pp. 714-718, 2007.
- [24] A. J. Menezes, P. C. van Oorschot, and S. A. Vanstone, "Handbook of Applied Cryptography," CRC Press, pp. 191-222, 1996.

Gamal M. Dousoky received his B.Sc. and M.Sc. in Electrical Engineering from Minia University, Minia, Egypt, in 2000 and 2004, respectively. He is currently working toward his Ph.D. in the Department of Electrical Engineering, Graduate School of Information Science and Electrical Engineering, Kyushu University, Fukuoka, Japan. Since 2000, he has been associated with the Department of Electrical Engineering, Faculty of Engineering at Minia University, first as a Teaching Assistant and, since 2004, as a Lecturer Assistant. His research interests include power electronics, especially renewable energy applications, switching power supplies, EMC/EMI, artificial intelligence, and digital control. He is a Student Member of IEICE, IEEE, IEEE Power Electronics Society (PELS), and IEEE Industrial Electronics Society (IES). Mr. Gamal received the 2009 Excellent Student Award from the IEEE Fukuoka Section.

Masahito Shoyama received his B. S. in Electrical Engineering and his Dr. Eng. from Kyushu University, Fukuoka, Japan, in 1981 and 1986, respectively. He joined the Dept. of Electronics, Kyushu University as a Research Associate in 1986, and he has been a Professor since 2010. Since 1996 he has been with the Dept. of Electrical and Electronic Systems Engineering of the Graduate School of Information Science and Electrical Engineering, Kyushu University. He has been active in the fields of power electronics, especially in high-frequency switching power supplies, power factor correctors, piezoelectric power converters, and electromagnetic compatibility (EMC). Dr. Shoyama is a member of IEEE, IEICE, IEEJ and SICE.

Tamotsu Ninomiya received his B.E., M.E., and Dr. Eng. in Electronics from Kyushu University, Fukuoka, Japan, in 1967, 1969, and 1981, respectively. Since 1969, he has been associated with the Department of Electronics, Kyushu University, first as a Research Assistant and since 1988 as a Professor. Since a reorganization in 1996, he has been a Professor in the Dept. of Electrical and Electronic Systems Engineering of the Graduate School of Information Science and Electrical Engineering. He has been a specialist in the field of power electronics. He served as General Chairman of PESC in 1998, and in January 2001, he was awarded as IEEE Fellow for contributions to the development of high-frequency switching power converters. He also served as Chairman of the Technical Group on Power Engineering in Electronics and Communications of the IEICE, and an Associate Editor of IEICE Transactions on Communications. Currently he is a TDK Endowed Chair Professor at Faculty of Engineering, Nagasaki University.