New Three-Level PWM DC/DC Converter – Analysis, Design and Experiments

Bor-Ren Lin[†] and Chih-Chieh Chen^{*}

^{†*}Dept. of Electrical Eng., National Yunlin University of Science and Technology, Yunlin, Taiwan

Abstract

This paper studies a new three-level pulse-width modulation (PWM) resonant converter for high input voltage and high load current applications. In order to use high frequency power MOSFETs for high input voltage applications, a three-level DC converter with two clamped diodes and a flying capacitor is adopted in the proposed circuit. For high load current applications, the secondary sides of the proposed converter are connected in parallel to reduce the size of the magnetic core and copper windings and to decrease the current rating of the rectifier diodes. In order to share the load current and reduce the switch counts, three resonant converters with the same active switches are adopted in the proposed circuit. Two transformers with a series connection in the primary side and a parallel connection in the secondary side are adopted in each converter to balance the secondary side currents. To overcome the drawback of a wide range of switching frequencies in conventional series resonant converters, the duty cycle control is adopted in the proposed circuit to achieve zero current switching (ZCS) turn-off for the rectifier diodes and zero voltage switching (ZVS) turn-on for the active switches. Finally, experimental results are provided to verify the effectiveness of the proposed converter.

Key words: DC/DC converter, PWM

I. INTRODUCTION

For three-phase 380V or 480V systems, an AC/DC converter with power factor correction (PFC) is needed in the front stage for reducing current harmonics at the utility side in order to meet international standards (IEC 61000-3-2 or IEEE 519). Thus, the DC bus voltage after the AC/DC converter is greater than 540V or 680V. In order to use MOSFETs instead of IGBTs in the second DC/DC converter stage with a high switching frequency and high power density demand, three-level circuit topologies [1]-[4] have been proposed for high input voltage and medium/high power applications. Soft switching three-level converters have been presented in [5]-[10] to reduce the switching losses at a desired load range. These techniques are based on an additional auxiliary circuit to extend the zero voltage switching (ZVS) range or using the leakage inductance (or external inductance) and the output capacitance of the MOSFETs to turn on the active switches under ZVS. However, the rectifier diodes at the secondary side have

reverse recovery losses. Series resonant converters [11]-[16] have been proposed to have the features of ZVS turn-on for power switches and ZCS turn-off for rectifier diodes within a wide range of input voltage and load conditions when the switching frequency is less than the series resonant frequency. The main drawback of series resonant converters is the wide range of switching frequencies from light load to full load. Thus, the magnetic components in the circuit are not easy to design at the optimal condition. In order to keep the advantages of series resonant converters and operate at a fixed switching frequency, the resonant converter has a better ability to operate at duty cycle control with soft switching features such as ZVS for the MOSFETs and ZCS for the fast recovery diodes. For high load current applications such as high power battery chargers, parallel three-level converters are normally adopted.

This paper proposes a new three-level PWM resonant converter with ZVS/ZCS for high input voltage and high load current applications. A three-level DC converter with two clamped diodes and one flying capacitor is used to limit the voltage stress of the power switches at $V_{in}/2$. Three PWM resonant converters with the same power switches are used to share the load current for high load current applications. Thus, the switch counts in the proposed circuit are reduced when compared with conventional parallel three-level DC/DC

Manuscript received May 24, 2013; revised Oct. 30, 2013

Recommended for publication by Associate Editor Joung-Hu Park.

[†]Corresponding Author: linbr@yuntech.edu.tw

Tel: +886-5-5516128, Fax: +886-5-5312065, Nat'l Yunlin Univ. of Sci. & Tech.

^{*}Dept. of Electrical Eng., National Yunlin University of Science and Technology, Taiwan

Fig. 1. Circuit configuration of the proposed resonant converter.

converters. A series resonant converter is adopted in the transformer primary side and the switching frequency is less than the series resonant frequency. Thus, all of the active switches are turned on under ZVS and the rectifier diodes are turned off under ZCS. Duty cycle control instead of frequency modulation (FM) control is adopted to regulate the output voltage. Thus, the drawback of a wide range of switching frequencies in conventional resonant converters is overcome. Finally, experiments are provided to verify the operation principle of the proposed converter.

II. CIRCUIT CONFIGURATION

The circuit configuration of the proposed converter is shown in Fig. 1 for medium/high input voltage and high load current applications. The proposed circuit includes three ZVS DC converters connected in parallel. The first DC converter consists of C_{in1} , C_{in2} , D_a , D_b , C_f , S_1 - S_4 , C_1 - C_4 , C_{r1} , L_{r1} , T_1 - T_2 , D_1 - D_4 , C_o and R_o . The second DC converter includes the components of C_{in1} , C_{in2} , D_a , D_b , C_f , S_1 - S_4 , C_1 - C_4 , C_{r2} , L_{r2} , T_3 - T_4 , D_5 - D_8 , C_o and R_o . In the same manner, the components C_{in1} , C_{in2} , D_a , D_b , C_f , S_1 - S_4 , C_1 - C_4 , C_{r3} , L_{r3} , T_5 - T_6 , D_9 - D_{12} , C_o and R_o are included in the third DC converter. The input capacitances, C_{in1} and C_{in2} , are equal and large enough to be two input voltage sources $v_{Cin1}=v_{Cin2}=V_{in}/2$. S_1 - S_4 are power MOSFETs with $V_{in}/2$ voltage stress. C_1 - C_4 are the output capacitances of S_1 - S_4 , respectively. D_a and D_b are the clamped diodes. C_f is a flying capacitor with $V_{in}/2$ average voltage. C_{r1} - C_{r3} are the series resonant capacitors, and L_{r1} - L_{r3} are the series resonant inductances. L_{m1} - L_{m6} are the magnetizing inductances of T_1 - T_6 , respectively. D_1 - D_{12} are the rectifier diodes. R_o is the load resistance, and C_o is the output capacitance. These three DC converters share the same components in terms of S_1 - S_4 , D_a , D_b , and C_f . In each of the

DC converters, the two transformers are connected in series at the primary side and connected in parallel at the secondary side so that the two secondary side currents are balanced for high load current applications. The PWM signals of S_1 and S_4 are complementary each other with a dead time to allow for ZVS operation. Similarly, the PWM signals of S_2 and S_3 are complementary each other. Based on the operations of S_1 - S_4 , there are three voltage levels V_{in} , $V_{in}/2$ and 0 generated on the AC terminal voltages v_{ab} , v_{bc} and v_{bo} . Each center-tapped diode rectifier supplies one-sixth of the load current. Thus, the current stresses of each of the transformer secondary windings and the rectifier diodes are reduced.

III. OPERATION PRINCIPLE

The key waveforms of the proposed resonant converter are shown in Fig. 2. The duty cycle of the active switches S_1 - S_4 is equal to 0.5. The PWM signals of S_2 and S_3 are phase-shifted with respect to the PWM signals of S_1 and S_4 , respectively. The duty cycle of the AC side voltages v_{ab} , v_{bc} and v_{bo} is regulated to keep the output voltage at a desired value against load variations and input voltage changes. Before the system analysis, the following assumptions are made in the proposed converter. (1) V_{Cin1} and V_{Cin2} are balanced voltage sources; (2) $C_1=C_2=C_3=C_4 \equiv C_{oss}$, $C_{r1}=C_{r2}=C_{r3} \equiv C_r$ and $C_r > C_{oss}$; (3) the average capacitor voltages $V_{Cr3}=0$ and $V_{Cr1}=V_{Cr2}=V_{Cf}=V_{in}/2$; (4) V_o is the constant output voltage; (5) $L_{m1}=L_{m2}=L_{m3}=L_{m4}=L_{m5}=L_{m6} \equiv L_m$, $L_{r1}=L_{r2}=L_{r3} \equiv L_r$ and $L_r \ll L_m$; (6) the turns ratio of T_1 - T_6 is $n=n_p/n_{s1}=n_p/n_{s2}$; and (7) the MOSFETs, S_1 - S_4 , and diodes, D_1 - D_{12} and D_a - D_b , are ideal. Based on the on/off states of S_1 - S_4 , D_a - D_b and D_1 - D_{12} , the proposed converter has ten operating modes in a switching cycle. Fig. 3 gives the equivalent circuits of these operating modes. Prior to t_0 , S_1 is conducting. The inductor current i_{Lr1}

is positive and i_{Lr2} is negative.

Mode 1 [$t_0 \leq t_1$, Fig. 3(a)]: At t_0 , C_2 is discharged to zero voltage. Since $i_{Lr2}(t_0) + i_{Lr3}(t_0) - i_{Lr1}(t_0) < 0$, the anti-parallel diode of S_2 is conducting. Thus, S_2 can be turned on at this moment under ZVS. The AC terminal voltages $v_{ab}=0$, $v_{bc}=V_{in}$ and $v_{bo}=V_{in}/2$. Diodes D_2 , D_4 , D_5 , D_7 , D_9 and D_{11} are conducting in this mode. Magnetizing voltages $v_{Lm1}=v_{Lm2}=-nV_o$ and $v_{Lm3}=v_{Lm4}=v_{Lm5}=v_{Lm6}=nV_o$. Thus, i_{Lm1} and i_{Lm2} decrease and $i_{Lm3}-i_{Lm6}$ increase in this mode. L_{r1} and C_{r1} are resonant with the applied voltage $2nV_o$, L_{r2} and C_{r2} are resonant with the applied voltage $V_{in}-2nV_o$, and L_{r3} and C_{r3} are resonant with the applied voltage $V_{in}/2-2nV_o$. In this mode, $i_{Lr1}-i_{Lr3}$ and $v_{Cr1}-v_{Cr3}$ are expressed as:

$$i_{Lr1}(t) = \frac{2nV_o - v_{Cr1}(t_0)}{Z_1} \sin \omega_1(t-t_0) + i_{Lr1}(t_0) \cos \omega_1(t-t_0) \quad (1)$$

$$i_{Lr2}(t) = \frac{V_{in} - 2nV_o - v_{Cr2}(t_0)}{Z_1} \sin \omega_1(t-t_0) + i_{Lr2}(t_0) \cos \omega_1(t-t_0) \quad (2)$$

$$i_{Lr3}(t) = \frac{V_{in}/2 - 2nV_o - v_{Cr3}(t_0)}{Z_1} \sin \omega_1(t-t_0) + i_{Lr3}(t_0) \cos \omega_1(t-t_0) \quad (3)$$

$$v_{Cr1}(t) = 2nV_o - [2nV_o - v_{Cr1}(t_0)] \cos \omega_1(t-t_0) + i_{Lr1}(t_0) Z_1 \sin \omega_1(t-t_0) \quad (4)$$

$$v_{Cr2}(t) = V_{in} - 2nV_o - [V_{in} - 2nV_o - v_{Cr2}(t_0)] \cos \omega_1(t-t_0) + i_{Lr2}(t_0) Z_1 \sin \omega_1(t-t_0) \quad (5)$$

$$v_{Cr3}(t) = V_{in}/2 - 2nV_o - [V_{in}/2 - 2nV_o - v_{Cr3}(t_0)] \cos \omega_1(t-t_0) + i_{Lr3}(t_0) Z_1 \sin \omega_1(t-t_0) \quad (6)$$

where $Z_1 = \sqrt{L_r/C_r}$ and $\omega_1 = 1/\sqrt{L_r C_r}$. In this mode,

i_{Lr1} and v_{Cr1} are both decreasing, and $i_{Lr2}-i_{Lr3}$ and $v_{Cr2}-v_{Cr3}$ are increasing. Power is transferred from V_{in} to R_o through S_1 , S_2 , T_3 - T_6 , L_{r2} - L_{r3} , C_{r2} - C_{r3} , D_5 , D_7 , D_9 , D_{11} and C_o .

Mode 2 [$t_1 \leq t_2$, Fig. 3(b)]: At t_1 , S_1 is turned off. Since $i_{Lr2}(t_1)$ and $i_{Lr3}(t_1)$ are positive and $i_{Lr1}(t_1)$ is negative, C_1 is charged linearly and C_4 is discharged linearly. The rising slope of the drain-to-source voltage of S_1 is limited by C_1 and C_4 . Thus, S_1 is turned off under ZVS. Capacitor C_4 can be discharged to zero voltage if the energy stored in L_{r1} - L_{r3} is greater than the energy stored in C_1 and C_4 . Therefore, the ZVS condition of S_4 is expressed as:

$$L_r[i_{Lr1}^2(t_1) + i_{Lr2}^2(t_1) + i_{Lr3}^2(t_1)] \geq C_{oss} V_{in}^2/2 \quad (7)$$

Mode 3 [$t_2 \leq t_3$, Fig. 3(c)]: At t_2 , C_4 is discharged to zero voltage. Since $i_{Lr2}(t_2)$ and $i_{Lr3}(t_2)$ are positive and $i_{Lr1}(t_2)$ is negative, the anti-parallel diode of S_4 is conducting. Thus, S_4 is turned on at this moment under ZVS. The AC terminal voltages $v_{ab}=v_{bc}=V_{in}/2$ and $v_{bo}=0$. Since diodes D_2 , D_4 , D_5 , D_7 , D_9 and D_{11} are still conducting, the magnetizing currents i_{Lm1} and i_{Lm2} decrease and $i_{Lm3}-i_{Lm6}$ increase in this mode. L_{r1} and C_{r1} are resonant with the applied voltage $V_{in}/2+2nV_o$. In the same manner, L_{r2} and C_{r2} are resonant with the applied

Fig. 2. Key waveforms of the proposed converter.

voltage $V_{in}/2-2nV_o$, and L_{r3} and C_{r3} are resonant with the applied voltage $-2nV_o$. In this mode, $i_{Lr1}-i_{Lr3}$ and $v_{Cr1}-v_{Cr3}$ are given as:

$$i_{Lr1}(t) = \frac{V_{in}/2 + 2nV_o - v_{Cr1}(t_2)}{Z_1} \sin \omega_1(t-t_2) + i_{Lr1}(t_2) \cos \omega_1(t-t_2) \quad (8)$$

$$i_{Lr2}(t) = \frac{V_{in}/2 - 2nV_o - v_{Cr2}(t_2)}{Z_1} \sin \omega_1(t-t_2) + i_{Lr2}(t_2) \cos \omega_1(t-t_2) \quad (9)$$

$$i_{Lr3}(t) = \frac{-2nV_o - v_{Cr3}(t_2)}{Z_1} \sin \omega_1(t-t_2) + i_{Lr3}(t_2) \cos \omega_1(t-t_2) \quad (10)$$

$$v_{Cr1}(t) = V_{in}/2 + 2nV_o - [V_{in}/2 + 2nV_o - v_{Cr1}(t_2)] \cos \omega_1(t-t_2) + i_{Lr1}(t_2) Z_1 \sin \omega_1(t-t_2) \quad (11)$$

$$v_{Cr2}(t) = V_{in}/2 - 2nV_o - [V_{in}/2 - 2nV_o - v_{Cr2}(t_2)] \cos \omega_1(t-t_2) + i_{Lr2}(t_2) Z_1 \sin \omega_1(t-t_2) \quad (12)$$

$$v_{Cr3}(t) = -2nV_o + [2nV_o + v_{Cr3}(t_2)] \cos \omega_1(t-t_2) + i_{Lr3}(t_2) Z_1 \sin \omega_1(t-t_2) \quad (13)$$

The flying capacitor voltage $v_{Cf}=v_{Cin2}=V_{in}/2$.

Mode 4 [$t_3 \leq t < t_4$, Fig. 3(d)]: At t_3 , $i_{Lm1}=i_{Lm2}=i_{Lr1}$, $i_{Lm3}=i_{Lm4}=i_{Lr2}$ and $i_{Lm5}=i_{Lm6}=i_{Lr3}$. Thus, diodes D_1 - D_{12} are all in the off-state. C_{r1} , L_{r1} , L_{m1} and L_{m2} are resonant with the applied voltage $V_{in}/2$. In the same manner, C_{r2} , L_{r2} , L_{m3} and L_{m4} are resonant with the applied voltage $V_{in}/2$, and C_{r3} , L_{r3} , L_{m5} and L_{m6} are resonant. In this mode, i_{Lr1} - i_{Lr3} and v_{Cr1} - v_{Cr3} are expressed as:

$$i_{Lr1}(t) = \frac{V_{in}/2 - v_{Cr1}(t_3)}{Z_2} \sin \omega_2(t - t_3) + i_{Lr1}(t_3) \cos \omega_2(t - t_3) \quad (14)$$

$$i_{Lr2}(t) = \frac{V_{in}/2 - v_{Cr2}(t_3)}{Z_2} \sin \omega_2(t - t_3) + i_{Lr2}(t_3) \cos \omega_2(t - t_3) \quad (15)$$

$$i_{Lr3}(t) = -\frac{v_{Cr3}(t_3)}{Z_2} \sin \omega_2(t - t_3) + i_{Lr3}(t_3) \cos \omega_2(t - t_3) \quad (16)$$

$$v_{Cr1}(t) = V_{in}/2 - [V_{in}/2 - v_{Cr1}(t_3)] \cos \omega_2(t - t_3) + i_{Lr1}(t_3) Z_2 \sin \omega_2(t - t_3) \quad (17)$$

$$v_{Cr2}(t) = V_{in}/2 - [V_{in}/2 - v_{Cr2}(t_3)] \cos \omega_2(t - t_3) + i_{Lr2}(t_3) Z_2 \sin \omega_2(t - t_3) \quad (18)$$

$$v_{Cr3}(t) = v_{Cr3}(t_3) \cos \omega_2(t - t_3) + i_{Lr3}(t_3) Z_2 \sin \omega_2(t - t_3) \quad (19)$$

where $Z_2 = \sqrt{\frac{(L_r + 2L_m)}{C_r}}$ and $\omega_2 = \frac{1}{\sqrt{(L_r + 2L_m)C_r}}$.

Mode 5 [$t_4 \leq t < t_5$, Fig. 3(e)]: At t_4 , S_2 is turned off. Since $i_{Lr2}(t_4)$ and $i_{Lr3}(t_4)$ are positive and $i_{Lr1}(t_4)$ is negative, C_2 is charged and C_3 is discharged linearly. The rising slope of the drain-to-source voltage of S_2 is limited by C_2 and C_3 . Thus, S_2 is turned off under ZVS. Capacitor C_3 can be discharged to zero voltage if the energy stored in L_{r1} - L_{r3} and L_{m1} - L_{m6} is greater than the energy stored in C_2 and C_3 . Therefore, the ZVS condition of S_3 is given as:

$$(L_r + 2L_m)[i_{Lr1}^2(t_4) + i_{Lr2}^2(t_4) + i_{Lr3}^2(t_4)] \geq C_{oss} V_{in}^2 / 2 \quad (20)$$

Mode 6 [$t_5 \leq t < t_6$, Fig. 3(f)]: At t_5 , C_3 is discharged to zero voltage. Since $i_{Lr2}(t_5)$ and $i_{Lr3}(t_5)$ are positive and $i_{Lr1}(t_5)$ is negative, the anti-parallel diode of S_3 is conducting. Thus, S_3 is turned on at this moment under ZVS. The AC terminal voltages $v_{ab}=V_{in}$, $v_{bc}=0$ and $v_{bo}=-V_{in}/2$. Diodes D_1 , D_3 , D_6 , D_8 , D_{10} and D_{12} are conducting in this mode. Thus, the magnetizing voltages $v_{Lm1}=v_{Lm2}=nV_o$ and $v_{Lm3}=v_{Lm4}=v_{Lm5}=v_{Lm6}=-nV_o$ so that i_{Lm1} and i_{Lm2} increase and i_{Lm3} - i_{Lm6} decrease. L_{r1} and C_{r1} are resonant with the applied voltage $V_{in}-2nV_o$. In the same manner, L_{r2} and C_{r2} are resonant with the applied voltage $2nV_o$, and L_{r3} and C_{r3} are resonant with the applied voltage $-V_{in}/2+2nV_o$.

Mode 7 [$t_6 \leq t < t_7$, Fig. 3(g)]: At t_6 , S_4 is turned off. Since $i_{Lr2}(t_6)$ and $i_{Lr3}(t_6)$ are negative and $i_{Lr1}(t_6)$ is positive, C_1 is discharged linearly and C_4 is charged linearly. The rising slope of the drain-to-source voltage of S_4 is limited by C_1 and C_4 so that S_4 is turned off under ZVS. Capacitor C_1 can be discharged to zero voltage if the energy stored in L_{r1} - L_{r3} is greater than the energy stored in C_1 and C_4 . Thus, the ZVS

condition of S_1 is given as:

$$L_r[i_{Lr1}^2(t_6) + i_{Lr2}^2(t_6) + i_{Lr3}^2(t_6)] \geq C_{oss} V_{in}^2 / 2 \quad (21)$$

Mode 8 [$t_7 \leq t < t_8$, Fig. 3(h)]: At t_7 , capacitor C_1 is discharged to zero voltage. Since $i_{Lr2}(t_7)$ and $i_{Lr3}(t_7)$ are negative and $i_{Lr1}(t_7)$ is positive, the anti-parallel diode of S_1 is conducting. S_1 is turned on at this moment under ZVS. The AC terminal voltages $v_{ab}=v_{bc}=V_{in}/2$ and $v_{bo}=0$. Since diodes D_1 , D_3 , D_6 , D_8 , D_{10} and D_{12} are still conducting, i_{Lm1} and i_{Lm2} increase and i_{Lm3} - i_{Lm6} decrease. L_{r1} and C_{r1} are resonant with the applied voltage $V_{in}/2-2nV_o$. In the same manner, L_{r2} and C_{r2} are resonant with the applied voltage $V_{in}/2+2nV_o$, and L_{r3} and C_{r3} are resonant with the applied voltage $2nV_o$ in this mode. The flying capacitor voltage $v_{Cf}=v_{Cin1}=V_{in}/2$.

Mode 9 [$t_8 \leq t < t_9$, Fig. 3(i)]: At t_8 , $i_{Lm1}=i_{Lm2}=i_{Lr1}$, $i_{Lm3}=i_{Lm4}=i_{Lr2}$ and $i_{Lm5}=i_{Lm6}=i_{Lr3}$. Thus, D_1 - D_{12} are all in the off-state. C_{r1} , L_{r1} , L_{m1} and L_{m2} are resonant with the applied voltage $V_{in}/2$. Similarly, C_{r2} , L_{r2} , L_{m3} and L_{m4} are resonant with the applied voltage $V_{in}/2$, and C_{r3} , L_{r3} , L_{m5} and L_{m6} are resonant in this mode.

Mode 10 [$t_9 \leq t < t_0$, Fig. 3(j)]: At t_9 , S_3 is turned off. Since $i_{Lr2}(t_9)$ and $i_{Lr3}(t_9)$ are negative and $i_{Lr1}(t_9)$ is positive, C_2 is discharged and C_3 is charged linearly. The rising slope of the drain-to-source voltage of S_3 is limited by C_2 and C_3 so that S_3 is turned off under ZVS. Capacitor C_2 can be discharged to zero voltage if the energy stored in L_{r1} - L_{r3} and L_{m1} - L_{m6} is greater than the energy stored in C_2 and C_3 . The ZVS condition of S_2 is given as:

$$(L_r + 2L_m)[i_{Lr1}^2(t_9) + i_{Lr2}^2(t_9) + i_{Lr3}^2(t_9)] \geq C_{oss} V_{in}^2 / 2 \quad (22)$$

At t_0 , C_2 is discharged to zero voltage and the anti-parallel diode of S_2 is conducting. Then, the operations of the proposed converter in a switching cycle are complete.

IV. CIRCUIT CHARACTERISTICS

Since the time intervals in modes 2, 5, 7 and 10 are much less than the time periods in the other modes, only modes 1, 3, 4, 6, 8 and 9 are discussed in this section in order to derive the circuit characteristics of the proposed converter. In modes 1, 3, 6 and 8, the proposed converter is resonant at the series resonant frequency f_r by L_r and C_r . In modes 4 and 9, the converter is resonant at the frequency $f_m = 1/2\pi\sqrt{(L_r + 2L_m)C_r}$. Since a quasi square voltage waveform is generated at the AC terminal voltages v_{ab} , v_{bc} and v_{bo} , the maximum duty ratio of v_{ab} , v_{bc} and v_{bo} is equal to 0.5. Thus, the AC voltage gain of the proposed resonant converter with a maximum duty ratio of 0.5 can be expressed in (23) based on the fundamental frequency analysis.

$$|G_{ac}(f_s)| = \frac{2V_{Lm,f}}{V_{ab,f}} \quad (23)$$

$$= 1/\sqrt{[1 + k(1 - (f_r^2/f_s^2))]^2 + Q^2[(f_s/f_r) - (f_r/f_s)]^2}$$

Fig. 3. Operation modes of the proposed converter during one switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8 (i) mode 9 (j) mode 10.

where $k=L_r/(2L_m)$, $R_{ac}=48n^2R_o/\pi^2$, $f_r=1/2\pi\sqrt{L_rC_r}$, $Q=Z_o/(2R_{ac})=\sqrt{L_r/C_r}/(2R_{ac})$ and f_s is the switching frequency. The maximum DC voltage gain of the proposed converter can be obtained at the minimum input voltage case.

$$G_{dc,max}=4n(V_o+V_f)/V_{in,min} \quad (24)$$

where V_f is the voltage drop on D_1 - D_{12} . If the duty ratio of the AC terminal voltages v_{ab} , v_{bc} and v_{bo} is less than 0.5, then the DC voltage gain of the proposed converter is less than $G_{dc,max}$. The DC voltage gain of the proposed converter is a nonlinear function of the duty cycle of the AC terminal voltages, the initial resonant inductor current and the initial resonant capacitor voltage. Thus, it is difficult to obtain the voltage conversion ratio in a closed form at the steady state. If the duty cycle of the AC terminal voltages is equal to 0.5, then the AC voltage gain of the proposed converter at the switching frequency can be obtained from (23) with the given parameters k , Q , f_s and f_r . Therefore, the necessary turns ratio of the isolated transformers T_1 - T_6 is expressed as:

$$n = \frac{G_{dc,max}V_{in,min}}{4(V_o+V_f)} = \frac{G_{ac}(f_s)V_{in,min}}{4(V_o+V_f)} \quad (25)$$

$$= \frac{V_{in,min}}{4(V_o+V_f)\sqrt{[1+k(1-(f_r^2/f_s^2))]^2+Q^2[(f_s/f_r)-(f_r/f_s)]^2}}$$

Since the selected switching frequency f_s is less than the series resonant frequency f_r in the resonant tank, the active switches S_1 - S_4 can be turned on under ZVS and the rectifier diodes can be turned off under ZCS. If the duty cycle of the AC terminal voltages v_{ab} , v_{bc} and v_{bo} is equal to 0.5, the peak magnetizing current I_m can be expressed as:

$$I_m = n(V_o+V_D)/(4L_m f_r) \quad (26)$$

Since $|i_{Lr1}(t_4)|=|i_{Lr2}(t_4)|=|i_{Lr3}(t_4)|=I_m$, the minimum resonant inductance to achieve ZVS turn-on for S_1 - S_4 can be obtained from (7), (20) and (26).

$$L_{r,min} = \max\left[\frac{C_{oss}V_{in}^2}{2[i_{Lr1}^2(t_1)+i_{Lr2}^2(t_1)+i_{Lr3}^2(t_1)]}, \frac{8C_{oss}L_m^2f_r^2V_{in}^2}{3n^2(V_o+V_D)^2}-2L_m\right] \quad (27)$$

The average voltages of C_{r1} , C_{r2} and C_f are equal to $V_{in}/2$ and the average voltage of C_{r3} is equal to zero. The voltage stress

of the active switches is equal to $V_{in}/2$ in the proposed converter. The voltage stress and the average current of the rectifier diodes D_1 - D_{12} are equal to $2(V_o+V_f)$ and $I_o/12$, respectively.

V. DESIGN EXAMPLE AND EXPERIMENTAL RESULTS

In this section, a design example and test results are provided to demonstrate the converter performance. The circuit specifications of a scale-down laboratory prototype are: $V_{in}=550V$ - $600V$, $V_o=24V$, $I_{o,rate}=60A$, series resonant frequency $f_r=125kHz$, switching frequency $f_s=100kHz$, $k=0.14$ and $Q=0.2$. The designed maximum AC gain of the LLC converter is at the minimum input voltage and full load condition. If the input voltage is increased or the output load is decreased, then the duty cycle is decreased. Thus, a normal duty cycle control PWM IC can be used to regulate the output voltage. Therefore, the requirement turns ratio of T_1 - T_6 can be obtained under the minimum input voltage case.

$$n = \frac{V_{in,min}}{4(V_o+V_f)\sqrt{[1+k(1-\frac{f_r^2}{f_s^2})]^2+Q^2(\frac{f_s}{f_r}-\frac{f_r}{f_s})^2}} \approx 6 \quad (28)$$

The primary and secondary winding turns of T_1 - T_6 are 30 turns and 5 turns, respectively. The AC equivalent resistance R_{ac} at full load is obtained as:

$$R_{ac} = 48n^2R_o/\pi^2 = 48 \times 6^2 \times (24/60)/3.14159^2 \approx 70\Omega \quad (29)$$

The series resonant inductance and the resonant capacitance are obtained as:

$$L_r = QR_{ac}/(\pi f_r) = \frac{0.2 \times 70}{\pi \times 125000} \approx 36\mu H \quad (30)$$

$$C_r = 1/(4\pi^2 L_r f_r^2) = 1/(4\pi^2 \times 36 \times 10^{-6} \times 125000^2) \approx 45nF \quad (31)$$

The magnetizing inductances of T_1 - T_6 are given as:

$$L_m = L_r/(2k) = 36/(2 \times 0.14) \approx 128\mu H \quad (32)$$

The selected flying capacitance C_f is $0.4\mu F$. The output

Fig. 4. Measured waveforms of the PWM signals of S_1 - S_4 at 20% load and (a) $V_{in}=550V$ (b) $V_{in}=600V$.

capacitance C_o is $4000\mu F$. The voltage stress of the power switches S_1 - S_4 is equal to 300V. In the laboratory, the commercially available MOSFET with at least 300V voltage stress for the power switches S_1 - S_4 is an IRFP460 which has 500V voltage stress and 20A current stress. The voltage stress and average current of the rectifier diodes D_1 - D_{12} are given as:

$$v_{D,max} = 2(V_o + V_f) = 2 \times (24 + 0.78) = 49.56V \quad (33)$$

$$i_{D,av} = I_{o,max} / 12 \approx 5A \quad (34)$$

Thus, 30CPQ150 fast recovery diodes with 150V voltage stress, 30A current stress and 0.78V voltage drop are used for D_1 - D_{12} . 30ETH06 fast recovery diodes with 600V voltage stress and 30A current stress are used for the clamped diodes D_a and D_b . A UCC3895 commercial PWM IC is adopted to generate the necessary gate signals and to regulate the output voltage at a desired voltage level.

Test results based on a scale-down prototype derived from the previous section are provided to verify the effectiveness of the proposed converter. The measured waveforms of the PWM signals of S_1 - S_4 at a 20% load with different input voltages are shown in Fig. 4. S_2 and S_3 are phase-shifted with respect to S_1 and S_4 , respectively. Fig. 5 gives the measured waveforms of the PWM signals of the active switches at a 100% load and with different input voltages.

Fig. 5. Measured waveforms of the PWM signals of S_1 - S_4 at 100% load and (a) $V_{in}=550V$ (b) $V_{in}=600V$.

The high input voltage has a greater phase-shift angle between S_1 and S_2 . The measured gate voltage, drain voltage and switch current of S_1 at a 7% load and with different input voltages are shown in Fig. 6. Similarly, the measured gate voltage, drain voltage and switch current of S_2 - S_4 at a 7% load and with different input voltages are given in Figs. 7-9, respectively. It is clear that S_1 - S_4 are all turned on under ZVS from 7% loads. The voltage stress of S_1 - S_4 is equal to $V_{in}/2$. Fig. 10 shows the measured results of the gate voltages of S_1 and S_2 and the resonant inductor currents i_{Lr1} - i_{Lr3} at a full load and different input voltage cases. The inductor currents i_{Lr2} and i_{Lr3} are in phase with each other. Fig. 11 give the test results of the gate voltages of S_1 and S_2 , the AC side voltages v_{ab} - v_{bo} and the resonant capacitor voltages v_{Cr1} - v_{Cr3} at full load and different input voltage cases. Three voltage levels are negated on the AC terminal voltages v_{ab} - v_{bo} . When switches S_1 and S_2 are both on, v_{Cr1} decreases and v_{Cr2} and v_{Cr3} increase. On the other hand, v_{Cr1} increases and v_{Cr2} and i_{Lr2} decrease when S_1 and S_2 are both off. Fig. 12 gives the measured output currents of the six center-tapped rectifiers at full load and different input voltages. It is clear that all of the diodes D_1 - D_8 are turned off under ZCS and that the output currents of the six center-tapped rectifiers are balanced. The output current issue is depended on the components L_{r1} - L_{r3} , C_{r1} - C_{r3} , T_1 - T_6 and D_1 - D_{12} . If all of the

Fig. 6. Measured results of the gate voltage, drain voltage and switch current of S_1 at 7% load and (a) $V_{in}=550V$ (b) $V_{in}=600V$.

Fig. 7. Measured results of the gate voltage, drain voltage and switch current of S_2 at 7% load and (a) $V_{in}=550V$ (b) $V_{in}=600V$.

Fig. 8. Measured results of the gate voltage, drain voltage and switch current of S_3 at 7% load and (a) $V_{in}=550V$ (b) $V_{in}=600V$.

components are identical, then the output currents of the six center-tapped rectifiers are balanced. If the components

Fig. 9. Measured results of the gate voltage, drain voltage and switch current of S_4 at 7% load and (a) $V_{in}=550V$ (b) $V_{in}=600V$.

Fig. 10. Measured results of the gate voltages of S_1 and S_2 and resonant inductor currents i_{Lr1} - i_{Lr3} at full load and (a) $V_{in}=550V$ (b) $V_{in}=600V$.

variation of L_{r1} - L_{r3} is less than 5%, then the current unbalanced is less than 3% based on the measured results. Fig. 13 gives the measured circuit efficiencies of the proposed converter at different load conditions and input voltage cases.

VI. CONCLUSION

Fig. 11. Measured results of the gate voltages of S_1 and S_2 , AC side voltages v_{ab} - v_{bo} and resonant capacitor voltages v_{Cr1} - v_{Cr3} at full load and (a) $V_{in}=550V$ (b) $V_{in}=600V$.

A new three-level PWM resonant converter is presented in this paper. Three resonant circuits with the same active switches are adopted in the proposed converter to share the load current. In order to reduce the current stress of the transformer windings and the rectifier diodes, six center-tapped rectifiers are connected in parallel at the secondary side for high load current applications. A three-level PWM converter is adopted to reduce the voltage stress of the active switches for high input voltage applications. The duty cycle PWM control is used to regulate the output voltage. Since the selected switching frequency is less than the series resonant frequency in terms of the series

Fig. 12. Measured output currents of six center-tapped rectifiers at full load and (a) $V_{in}=550V$ (b) $V_{in}=600V$.

Fig. 13. Measured circuit efficiencies of the proposed converter at different load conditions and input voltage cases.

resonant inductance and resonant capacitance, the power MOSFETs can be turned on under ZVS and the rectifier diodes can be turned off under ZCS. Thus, the switching losses on the power semiconductors are reduced. Finally, experiments based on a scale-down laboratory prototype are provided to verify the effectiveness of the proposed converter.

ACKNOWLEDGMENT

This project is partly supported by the National Science Council of Taiwan under Grant NSC 102-2221-E-224 -022

-MY3.

REFERENCES

- [1] H. Ertl, J. W. Kolar, and F. C. Zach, "Analysis of a multilevel multicell switch-mode power amplifier employing the flying-battery concept," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 4, pp. 816-823, 2002.
- [2] B. M. Song, R. McDowell, A. Bushnell, and J. Ennis, "A three-level dc-dc converter with wide-input voltage operation for hip-electricpower-distribution systems," *IEEE Trans. Plasma Sci.*, Vol. 32, No. 5, pp. 1856-1863, Oct. 2004.
- [3] J. P. Lee, B. D. Min, T. J. Kim, D. W. Yoo, and B. K. Lee, "A novel topology for photovoltaic series connected dc/dc converter with high efficiency under wide load range," in *Proc. IEEE Power Electron. Spec. Conf.*, pp. 152-155, 2007.
- [4] E. Deschamps and I. Barbi, "A flying-capacitor ZVS PWM 1.5 kW dc-to-dc converter with half of the input voltage across the switches," *IEEE Trans. Power Electron.*, Vol. 15, No. 5, pp. 855-860, Sep. 2000.
- [5] Bor-Ren Lin, "Analysis, Design and Implementation of a Soft Switching DC/DC Converter," *Journal of Power Electronics*, Vol. 13, No. 1, pp. 20-30, Jan. 2013.
- [6] F. Canales, P. M. Barbosa, and F. C. Lee, "A zero voltage and zero current switching three level dc/dc converter," *IEEE Trans. Power Electron.*, Vol. 17, No. 6, pp. 898-964, Nov. 2002.
- [7] T. T. Song, N. Huang, and A. Ioinovici, "A family of zero-voltage and zero-current-switching (ZVZCS) three-level dc-dc converters with secondary-assisted regenerative passive snubber," *IEEE Trans. Circuits Syst.*, Vol. 52, No. 11, pp. 2473-2481, Nov. 2005.
- [8] F. Liu, J. Yan, and X. Ruan, "Zero-voltage and zero-currents switching PWM combined three-level dc/dc converter," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 5, pp. 1644-1654, May 2010.
- [9] J. P. Rodrigues, S. A. Mussa, I. Barbi, and A. J. Perin, "Three-level zero-voltage switching pulse-width modulation DC-DC boost converter with active clamping," *IET Proc.-Power Electron.*, Vol. 3, No. 3, pp. 345-354, 2010.
- [10] B.-R. Lin, "Implementation of a ZVS three-level converter with series-connected transformers," *Journal of Power Electronics*, Vol. 13, No. 2, pp. 177-185, Mar. 2013.
- [11] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. of IEEE APEC*, Vol. 2, pp. 1108-1112, 2002.
- [12] X. Xie, J. Zhang, C. Zhao, Z. Zhao, and Z. Qian, "Analysis and optimization of LLC resonant converter with a novel over-current protection circuit," *IEEE Trans. Power Electron.*, Vol. 22, No. 2, pp. 435-443, Mar. 2007.
- [13] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, Vol. 24, No. 5, pp. 1321-1329, May 2009.
- [14] B. R. Lin and J. Y. Dong, "ZVS resonant converter with parallel-series transformer connection," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 7, pp. 2972-2979, Jul. 2011.
- [15] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Using LLC resonant converter for designing wide-range voltage source," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 5, pp. 1746-1756, May 2011.
- [16] B. R. Lin and S. F. Wu, "Implementation of a series resonant converter with series-parallel transformers," *IET Proceedings – Power Electronics*, Vol. 4, No. 8, pp. 919-926, 2011.

Bor-Ren Lin received his B.S. degree in Electronic Engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 1988, and his M.S. and Ph.D. degrees in Electrical Engineering from the University of Missouri-Columbia, Columbia, MO, USA, in 1990 and 1993, respectively. From 1991

to 1993, he was a Research Assistant with the Power Electronic Research Center, University of Missouri. Since 1993, he has been with the Department of Electrical Engineering, National Yunlin University of Science and Technology, Douliou, Taiwan, where he is currently a Distinguished Professor. He is an Associate Editor of the *Institution of Engineering and Technology Proceedings—Power Electronics* and the *Journal of Power Electronics*. His current research interests include power-factor corrections, multilevel converters, active power filters, and soft-switching converters. He has authored more than 200 published technical journal papers in the area of power electronics. Dr. Lin is an Associate Editor of the *IEEE Transactions on Industrial Electronics*. He was the recipient of Research Excellence Awards in 2004, 2005, 2007 and 2011 from the Engineering College and the National Yunlin University of Science and Technology. He received Best Paper Awards from the 2007 and 2011 IEEE Conference on Industrial Electronics and Applications, the Taiwan Power Electronics 2007 Conference, and the IEEE–Power Electronics and Drive Systems 2009 Conference.

Chih-Chieh Chen is currently working toward his M.S. degree in Electrical Engineering from the National Yunlin University of Science and Technology, Yunlin, Taiwan, ROC. His current research interests include the design and analysis of power factor correction techniques, switching mode power supplies and soft

switching converters.